LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8911EXB

MIPI® DSI/CSI Bridge to eDP

Datasheet

1. Features

- **Single-Port MIPI® DSI/CSI Receiver**
  - Compliant with D-PHY1.2, DSI1.3 and CSI1.3
  - 1 clock lane and 1~4 configurable data lanes
  - 80Mb/s~2.0Gb/s per data lane
  - Data lane input de-skew
  - Internal Rterm calibration with less than 5% error
  - Programmable equalization
  - Support Burst and Non-Burst Mode
  - Support RGB565、RGB666、Loosely RGB666、RGB888、RGB10bpc、RGB12bpc、YUV422 8bpc、YUV422 10bpc、YUV422 12bpc、YUV420 12bpp input
- **eDP1.4 Transmitter**
  - Compliant to VESA eDP1.4 standard
  - Support1/2/4 data lanes with 1.62Gbps(RBR) or 2.7Gbps(HBR).
  - Optional SSC 0.5% down-spreading output
  - Configurable output swing for optimized EMI
  - MCCS over AUX channel
- **Miscellaneous**
  - Single 1.8V supply power
  - Temperature range: −40°C to +85°C
  - Packaged in 6mm x 6mm QFN48

2. General Description

The Lontium LT8911EXB is MIPI®DSI/CSI to eDP converter with a single-port MIPI receiver which has 1 clock lane and 4 data lanes operating at maximum 2.0Gbps per data lane and a maximum input bandwidth of 8.0Gbps. The converter decodes the input MIPI RGB16/18/24/30/36bpp、YUV422 16/20/24bpp、YUV420 12bpp packets and converts the formatted video data stream to a single-link VESA eDP1.4 compliant output with 1/2/4configurable data lanes, supporting RBR(1.62Gbps) and HBR(2.7Gbps) link data rate. The build-in optional SSC function reduces EMI effect on EMI-concerned system application.

The LT8911EXB is fabricated in advanced CMOS process and implemented in a small outline 6mm x 6mm QFN48 at 0.5mm pitch package respectively. This package is RoHS compliant and specified to operate from −40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Personal media players
- Gaming

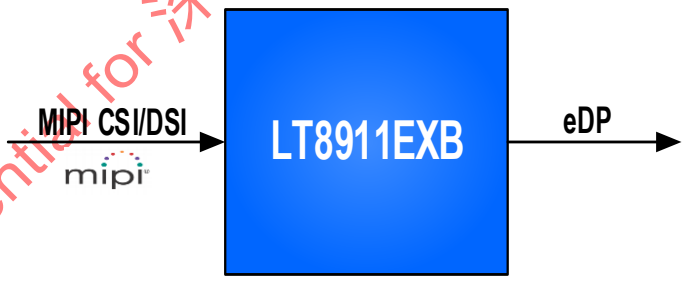


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method	MPQ
LT8911EXB	QFN48 (6*6)	−40°C to +85°C	Tray	4900pcs

Table of Contents

5. Revision History

Version	Owner	Content	Date(M/D/Y)
R1.0	XY J	Initial release	11/24/2017
	N W	Update package information	12/27/2017
R1.1	XY J	Update power consumption	11/05/2018
	N Wang	Update package information	11/15/2018
R1.2	XY J	Update ESD information	05/15/2019
R1.3	PP J	Update Figure 6.1.1	07/29/2019
R1.4	XY J	1.Update Features and General Description 2.Update Ordering Information 3.Update Pinning Information 4.Update Electrical Characteristics 5.Update Package Information	01/11/2022
R1.5	XY J	1.Update ESD information 2.Add TF package information	02/12/2022

6. Pinning Information

6.1 Pin Configuration

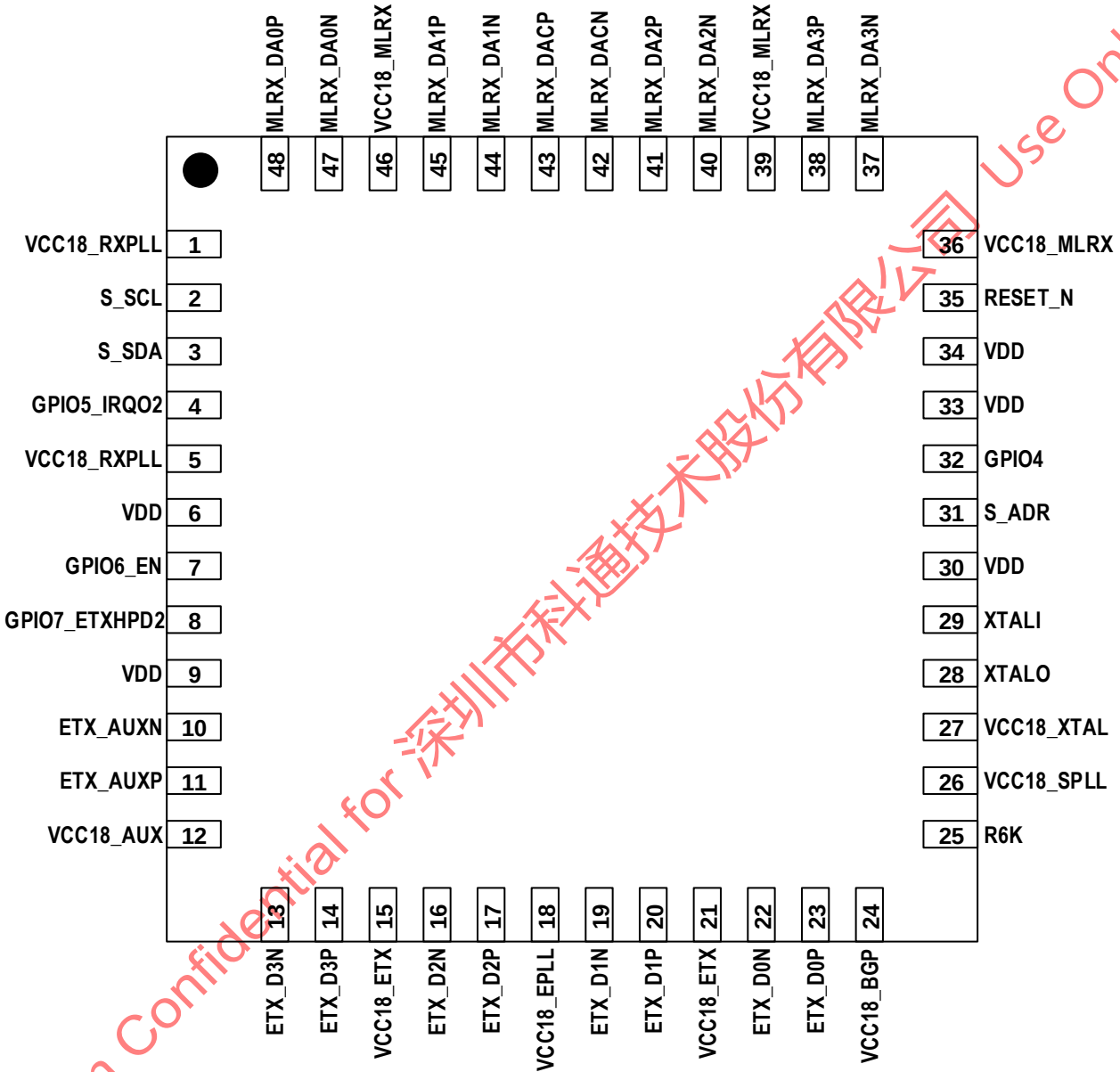


Figure 6.1.1 LT8911EXB QFN48 (6*6) Top View

6.2 Pin Description

Table 6.2.1 Pin Description

Pin No.	Pin Name	I/O Type	I/O Dir	Description
1	VCC18_RXPLL	PG	N/A	**RXPLL 1.8V Power** 1.8V power for RXPLL
2	S_SCL	OD	I/O	**I2C Data Clock** It serves as the serial port data clock slave for register access. Supports 1.8V CMOS logic.
3	S_SDA	OD	I/O	**I2C Data IO** It serves as the serial port data IO slave for register access. Supports 1.8V CMOS logic.
4	GPIO5_IRQO2	LVTTL,OD	I/O	**Interrupt Request Output** In default, this pin is configured as interrupt request (IRQ) output. **Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
5	VCC18_RXPLL	PG	N/A	**RXPLL 1.8V Power** 1.8V power for RXPLL
6	VDD	PG	N/A	**Digital core 1.8V Power** 1.8V power for digital core
7	GPIO6_EN	LVTTL,OD	I/O	**ChipEnable (High Active)** In default, this pin is configured as chip enable input. **Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
8	GPIO7_ETXHPD2	LVTTL,OD	I/O	**eDPTx HPD Control** In default, this pin is configured as eDPTX hot-plug detect input. **Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
9	VDD	PG	N/A	**Digital core 1.8V Power** 1.8V power for digital core
10	ETX_AUXN	Analog	I/O	**eDPTx AUX Channel Negative Output**
11	ETX_AUXP	Analog	I/O	**eDPTx AUX Channel Positive Output**
12	VCC18_AUX	PG	N/A	**eDPTx AUX Channel Power** 1.8V power for eDP AUX channel
13	ETX_D3N	Analog	O	**eDPTxPHY Data Lane-3 Negative Output** eDPTx output pin， data rate is up to 2.7Gb/s.
14	ETX_D3P	Analog	O	**eDPTxPHY Data Lane-3 Positive Output** eDPTx output pin， data rate is up to 2.7Gb/s.
15	VCC18_ETX	PG	N/A	**eDPTx PHY 1.8V Power** 1.8V power for eDPTx PHY
16	ETX_D2N	Analog	O	**eDPTxPHY Data Lane-2 Negative Output** eDPTx output pin， data rate is up to 2.7Gb/s.
17	ETX_D2P	Analog	O	**eDPTxPHY Data Lane-2 Positive Output** eDPTx output pin， data rate is up to 2.7Gb/s.
18	VCC18_EPLL	PG	N/A	**eDPTxPLL1.8V Power** 1.8V power for eDPTx PLL
19	ETX_D1N	Analog	O	**eDPTxPHY Data Lane-1 Negative Output** eDPTx output pin， data rate is up to 2.7Gb/s.
20	ETX_D1P	Analog	O	**eDPTxPHY Data Lane-1 Positive Output** eDPTx output pin， data rate is up to 2.7Gb/s.
21	VCC18_ETX	PG	N/A	**eDPTx PHY 1.8V Power** 1.8V power for eDPTxPHY
22	ETX_D0N	Analog	O	**eDPTxPHY Data Lane-0 Negative Output** eDPTx output pin， data rate is up to 2.7Gb/s.
23	ETX_D0P	Analog	O	**eDPTxPHY Data Lane-0 Positive Output**

Pin No.	Pin Name	I/O Type	I/O Dir	Description
				eDPTx output pin， data rate is up to 2.7Gb/s.
24	VCC18_BGP	PG	N/A	**Bandgap1.8V Power** 1.8V power for bandgap
25	R6K	Analog	O	**BandGap External Resistor** External 6K(±1%) resistor for setting internal reference current.
26	VCC18_SPLL	PG	N/A	**SYSPLL 1.8V Power** 1.8V power for System PLL
27	VCC18_XTAL	PG	N/A	**Crystal IO 1.8V Power** 1.8V power for Crystal IO
28	XTALO	LVTTL	O	**Crystal Clock Output** A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
29	XTALI	LVTTL	I	**Crystal Clock Input** A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock
30	VDD	PG	N/A	**Digital core 1.8V Power** 1.8V power for digital core
31	S_ADR	LVTTL	I	**I2C Device Address Select** It serves as the serial port address select. Supports 1.8V CMOS logic.
32	GPIO4	LVTTL	I/O	**Digital Test Signal Output** When this pin is configured as GPIO, it serves as digital test signal output.
33	VDD	PG	N/A	**Digital core 1.8V Power** 1.8V power for digital core
34	VDD	PG	N/A	**Digital core 1.8V Power** 1.8V power for digital core
35	RESET_N	LVTTL	I	**Hardware Reset Input** Chip reset signal, with internal 100k resister pullup.. Active LOW.
36	VCC18_MLRX	PG	N/A	**MIPI® D-PHY PHY Power** 1.8V power for MLRX
37	MLRX_DA3N	Analog	I	**MIPI® D-PHY Port-A Data Lane-3 Negative Input** Negative input of Uni-directional differential pairs up to 2.0Gb/s.
38	MLRX_DA3P	Analog	I	**MIPI® D-PHY Port-A Data Lane-3 Positive Input** Positive input of Uni-directional differential pairs up to 2.0Gb/s.
39	VCC18_MLRX	PG	N/A	**MIPI® D-PHY Power** 1.8V power for MLRX
40	MLRX_DA2N	Analog	I	**MIPI® D-PHY Data Lane-2 Negative Input** Negative input of Uni-directional differential pairs up to 2.0Gb/s.
41	MLRX_DA2P	Analog	I	**MIPI® D-PHY Data Lane-2 Positive Input** Positive input of Uni-directional differential pairs up to 2.0Gb/s.
42	MLRX_DACN	Analog	I	**MIPI® D-PHY Clock Lane Negative Input** Negative input of DDR clock differential pairs up to 1.0GHz in quadrature phase with data signals.
43	MLRX_DACP	Analog	I	**MIPI® D-PHY Clock Lane Positive Input** Positive input of DDR clock differential pairs up to 1.0GHz in quadrature phase with data signals.
44	MLRX_DA1N	Analog	I	**MIPI® D-PHY Data Lane-1 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 2.0Gb/s.
45	MLRX_DA1P	Analog	I	**MIPI® D-PHY Data Lane-1 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 2.0Gb/s.
46	VCC18_MLRX	PG	N/A	**MIPI® D-PHY Power** 1.8V power for MLRX

Pin No.	Pin Name	I/O Type	I/O Dir	Description
47	MLRX_DA0N	Analog	I	**MIPI® D-PHY Data Lane-0 Negative Input** Negative input of Uni-directional polarity swappable differential pairs up to 2.0Gb/s.
48	MLRX_DA0P	Analog	I	**MIPI® D-PHY Data Lane-0 Positive Input** Positive input of Uni-directional polarity swappable differential pairs up to 2.0Gb/s.

7. Function Block Diagram

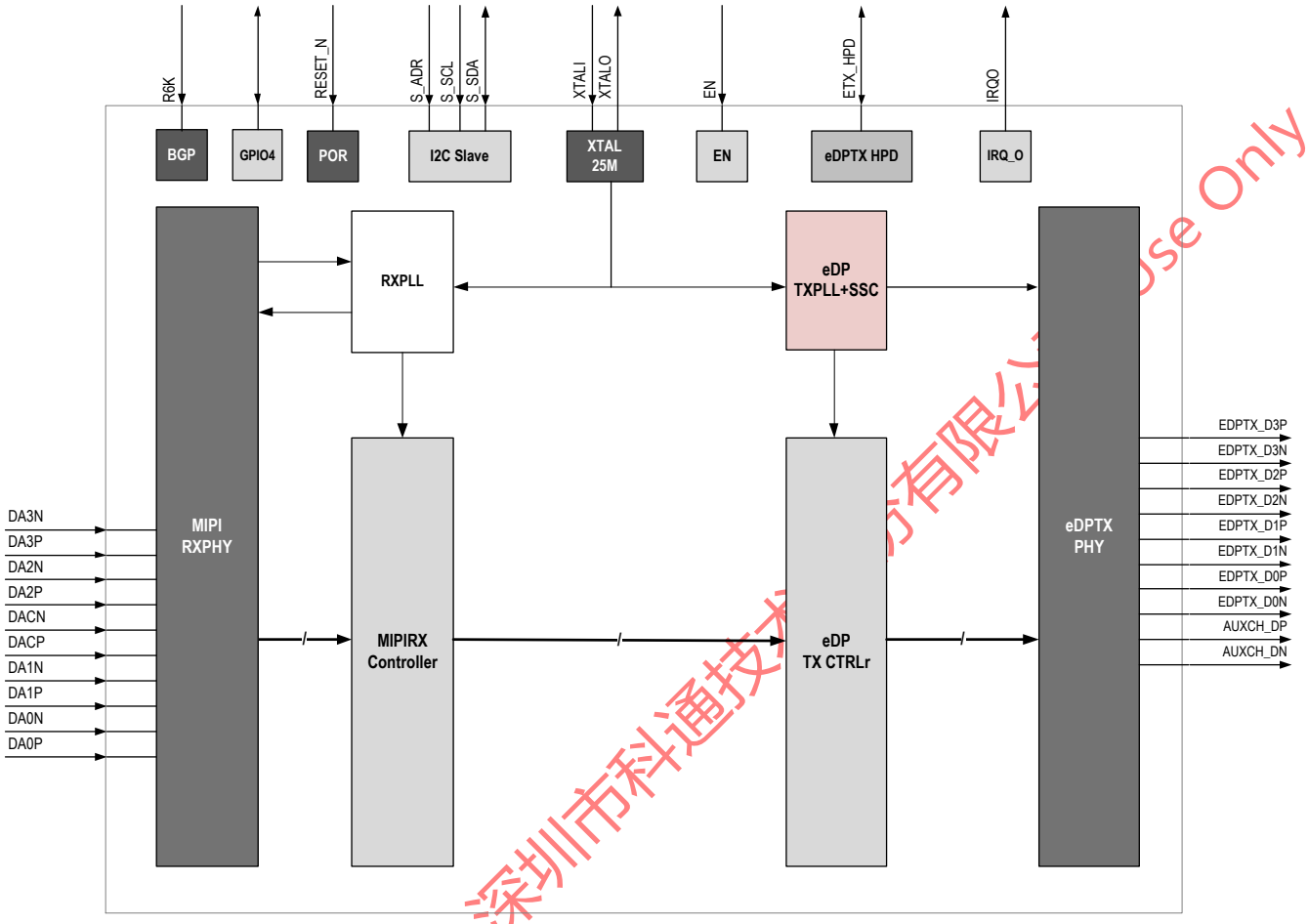


Figure 7.1 Function Block Diagram

8. Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC18_MLRX, VCC18_ETX, VCC18_SPLL, VCC18_XTAL, VCC18_BGP, VDD	1.8V Power Supply Voltage	-0.3		2.4	V
V_I	CMOS Terminal Input Voltage Range	-0.3		VDD+0.3	V
V_O	CMOS Terminal Output Voltage Range	-0.3		VDD+0.3	V
T_S	Storage Temperature	-40		125	℃
T_J	Junction Temperature			125	℃
ESD	HBM Electrostatic Discharge Level		±2000		V
	CDM Electrostatic Discharge Level		±250		V
Note: Permanent device damage may occur if absolute maximum conditions are exceeded.					

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC18_MLRX, VCC18_ETX, VCC18_SPLL, VCC18_XTAL, VCC18_BGP, VDD	1.8V Power Supply Voltage	1.62	1.8	1.98	V
T_A	Operating Free-air Temperature	-40	27	85	℃
θ_{JC}	Junction to Case Thermal Resistance		15.4		℃/W

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

MIPI HS Line Receiver DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{IDTH}	Differential input high voltage threshold			70	mV
V_{IDTL}	Differential input low voltage threshold	-70			mV
V_{IHHS}	Single ended input high voltage			460	mV
V_{ILHS}	Single ended input low voltage	-40			mV
$V_{CMRX(DC)}$	Input common mode voltage	70	200	330	mV
	Differential input impedance	80	100	125	Ω
MIPI LP Line Receiver DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV
V_{IH}	Input high voltage,data rate <=1.5Gbps	880			mV
	Input high voltage,data rate >1.5Gbps	740			mV
V_{HYST}	Input hysteresis	25			mV

eDP Transmitter DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{BIAS_TX}	TX DC Bias Voltage	1.62	1.8	1.98	V
$V_{tx\_diff\_vpp\_level0}$	Differential Peak to Peak Output Swing Level0	0.34	0.4	0.46	V
$V_{tx\_diff\_vpp\_level1}$	Differential Peak to Peak Output Swing Level1	0.51	0.6	0.68	V
$V_{tx\_diff\_vpp\_level2}$	Differential Peak to Peak Output Swing Level2	0.69	0.8	0.92	V
$V_{tx\_pre\_emp\_ratio}$	Pre-emphasis level 0	0	0	0	dB
	Pre-emphasis level 1	2.8	3.5	4.2	dB
	Pre-emphasis level 2	4.8	6	7.2	dB
	Pre-emphasis level 3	7.5	9.5	11.4	dB
C_{TX}	AC couple capacitance	75		200	nF
I_{TX_SHORT}	TX short circuit current limit			50	mA
R_{TX_DIFF}	Differential Impedance	80	100	120	Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

MIPI HS Line Receiver AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450MHz,data rate<=1.5Gbps			100	mV
	Common mode interference beyond 450MHz,data rate >1.5Gbps			50	mV
$\Delta V_{CMRX(LF)}$	Common mode interference between 50MHz and 450MHz,data rate <=1.5Gbps			100	mV
	Common mode interference between 50MHz and 450MHz,data rate>1.5Gbps.			50	mV
Ccm	Common mode termination			60	pF
MIPI LP Line Receiver AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
e_{SPIKE}	Input pulse rejection			300	V.ps
T_{MIN-RX}	Minimum pulse response	20			ns
V_{INT}	Peak interference voltage			200	mV
f_{INT}	Interference frequency	450			MHz
eDP Transmitter AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$T_{tx\_eye\_chip\_HBR}$	Minimum TX eye width at package pin	0.72			UI
$T_{tx\_jitter\_HBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pin			0.147	UI
$T_{tx\_eye\_chip\_RBR}$	Minimum TX eye width at package pin	0.82			UI
$T_{tx\_jitter\_RBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pin			0.09	UI
$T_{tx\_rise\_chip}$, $T_{tx\_fall\_chip}$	D+/D- TX output rise and fall time at TX package pins	50		130	ps
$T_{tx\_skew\_intra\_pair\_chip}$	Lane intra pair output skew at package pins			20	ps

$T_{tx\_rise\_fall\_mismatch\_chip}$	Lane intra pair rise and fall time mismatch at package pins			5	%

8.5 Power Consumption

Table 8.5.1 Power Consumption

Resolution	Input	Output	Power Consumption (mA)
1366x768	4-Lane MIPI	1-Lane/2.7G/Level3	204
1080P	4-Lane MIPI	2-Lane/2.7G/Level3	283
4K30			

8.6 Power-up and Reset Sequence

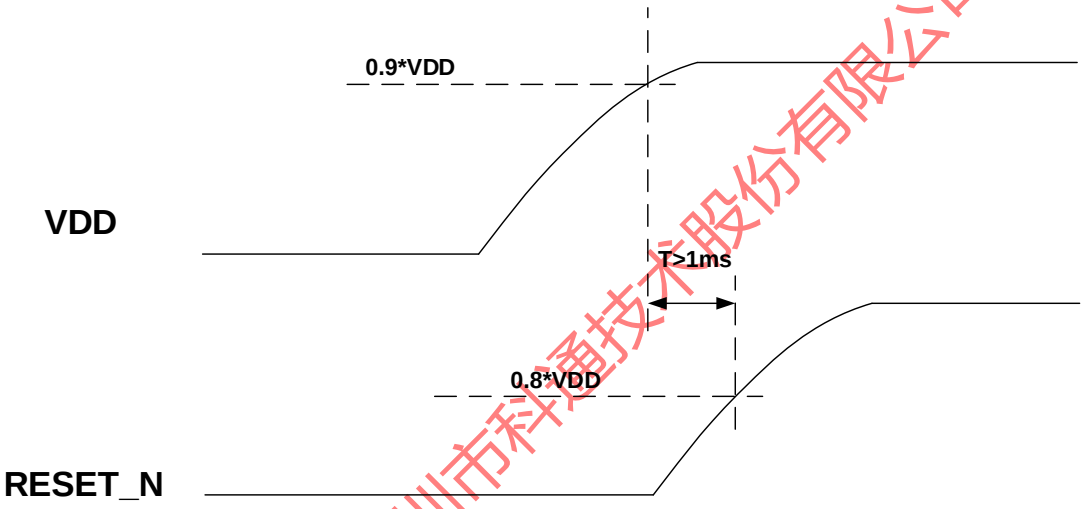
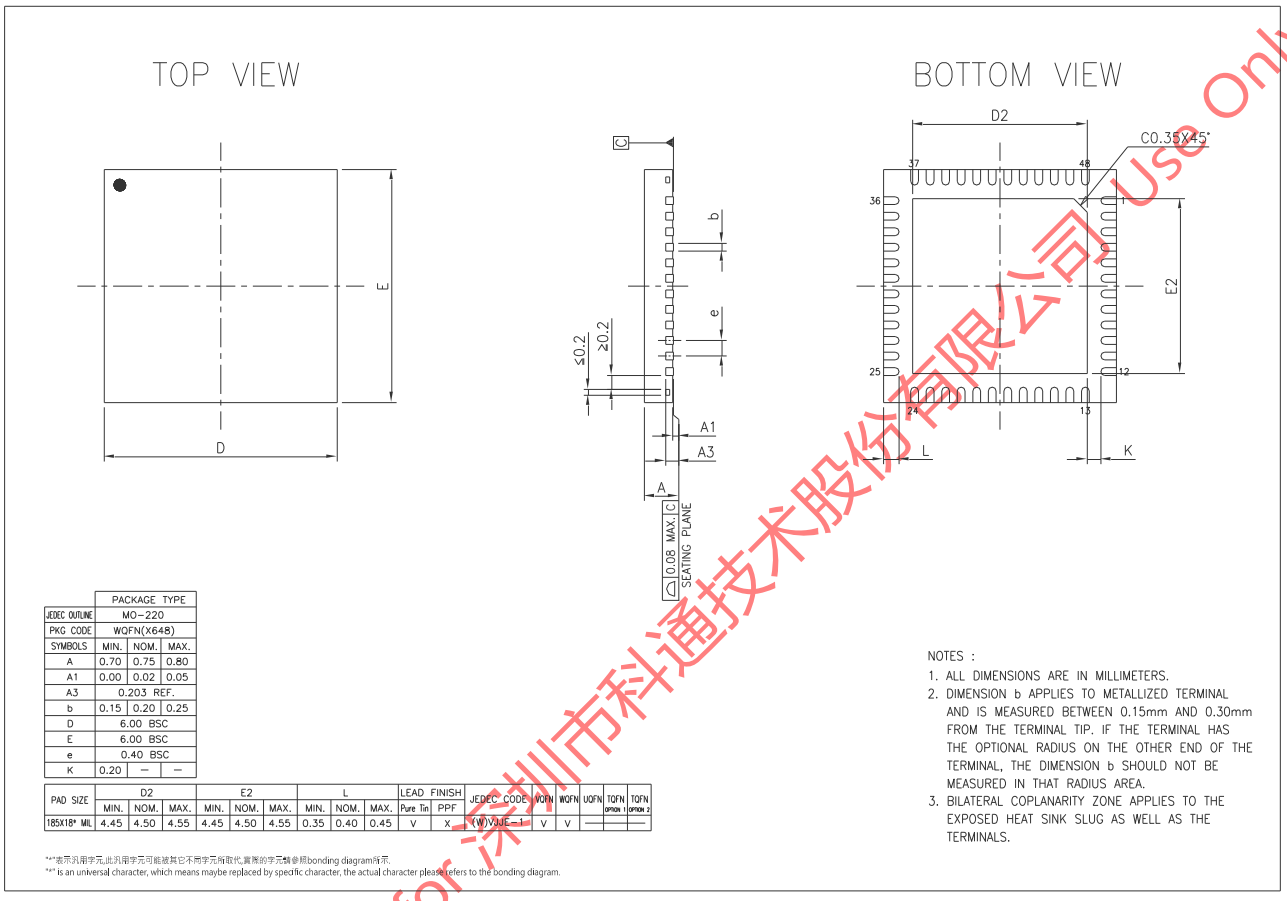


Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

9.1 Package Dimensions

Figure 9.1.1 is the package dimensions for the date code beginning with GT.
Figure 9.1.2 is the package dimensions for the date code beginning with TF.



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X648)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	–	–

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	WQFN	WQFN	UQFN	TQFN OPTION 1	TQFN OPTION 2
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
185X18* MIL	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	V	X	(W)VJJE-1	V	V			

*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 9.1.1 Package Dimensions (GT)

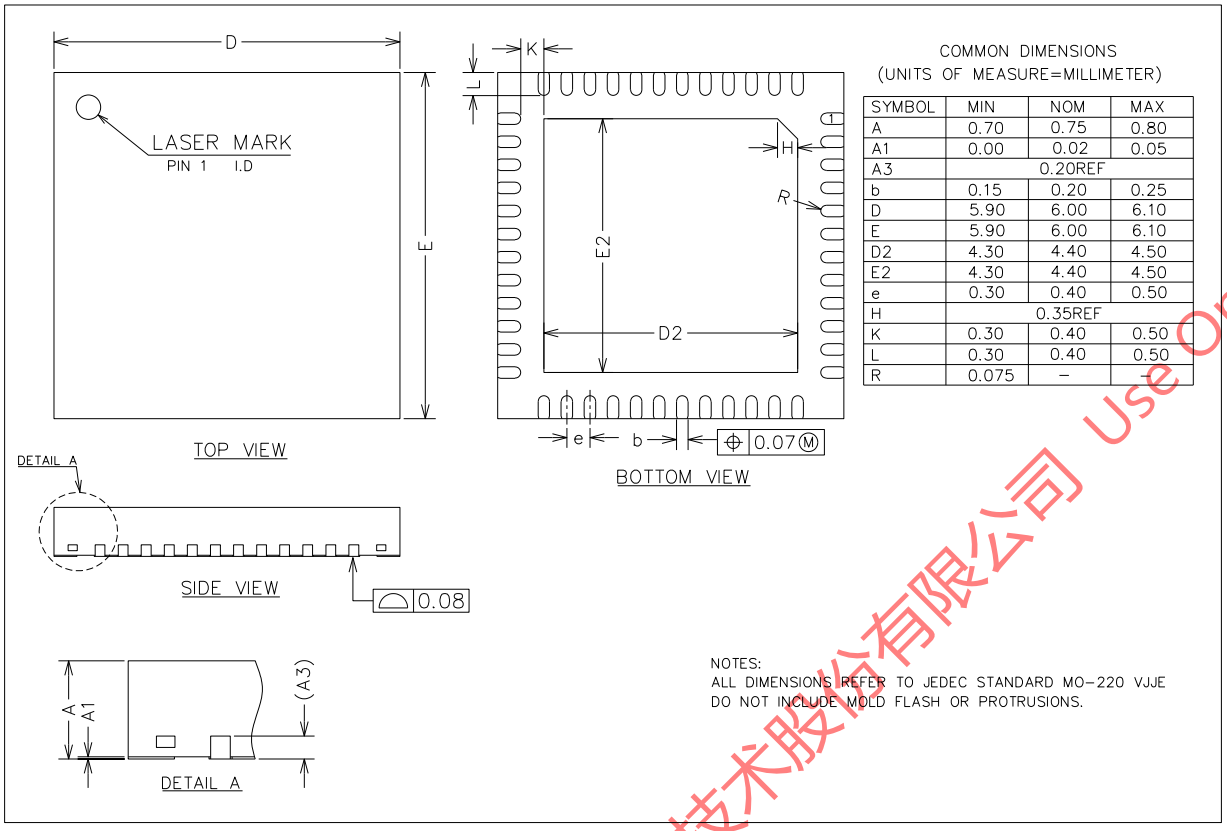


Figure 9.1.2 Package Dimensions (TF)

9.2 Packing Dimensions

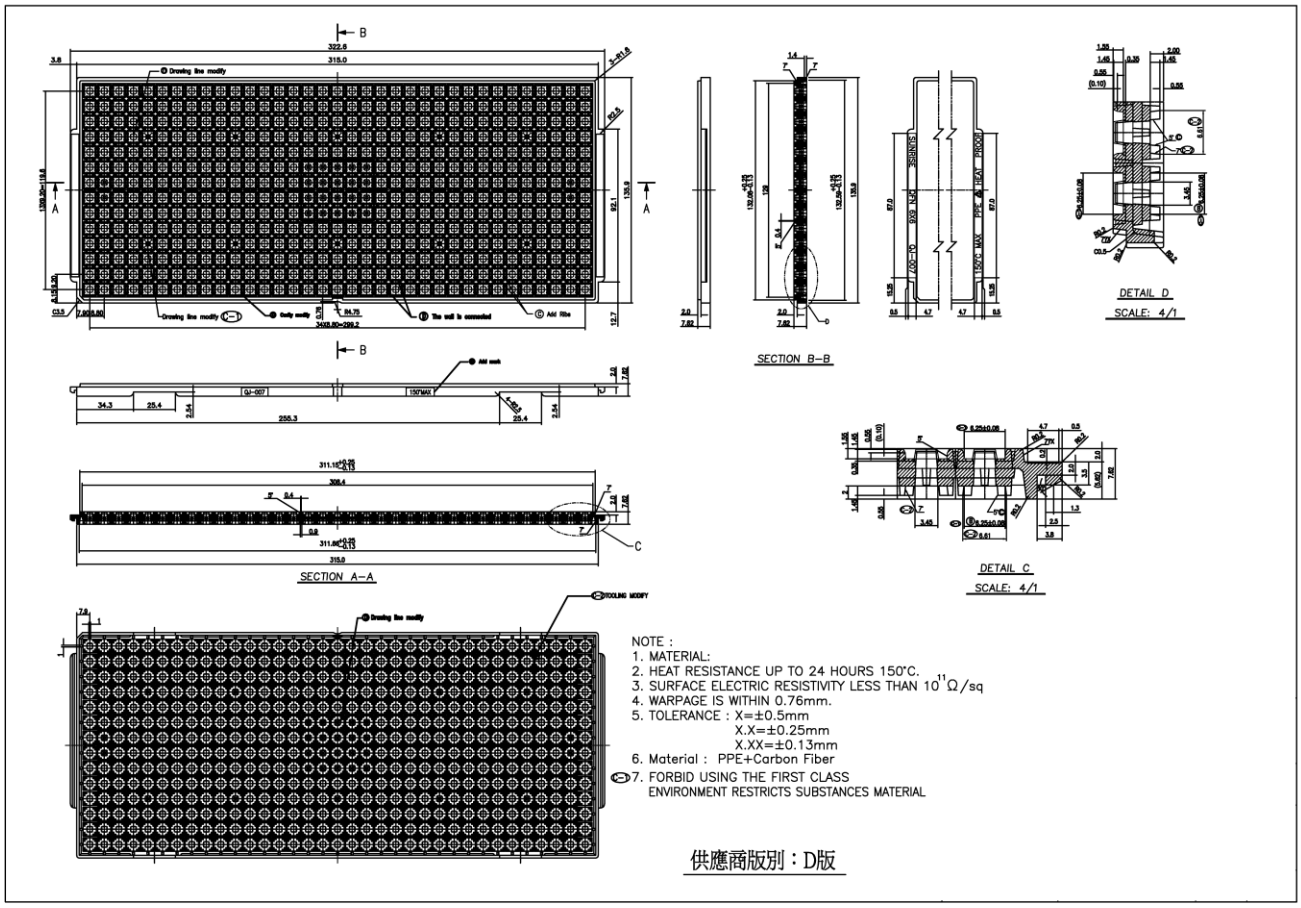


Figure 9.2.1 Packing Dimensions

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com