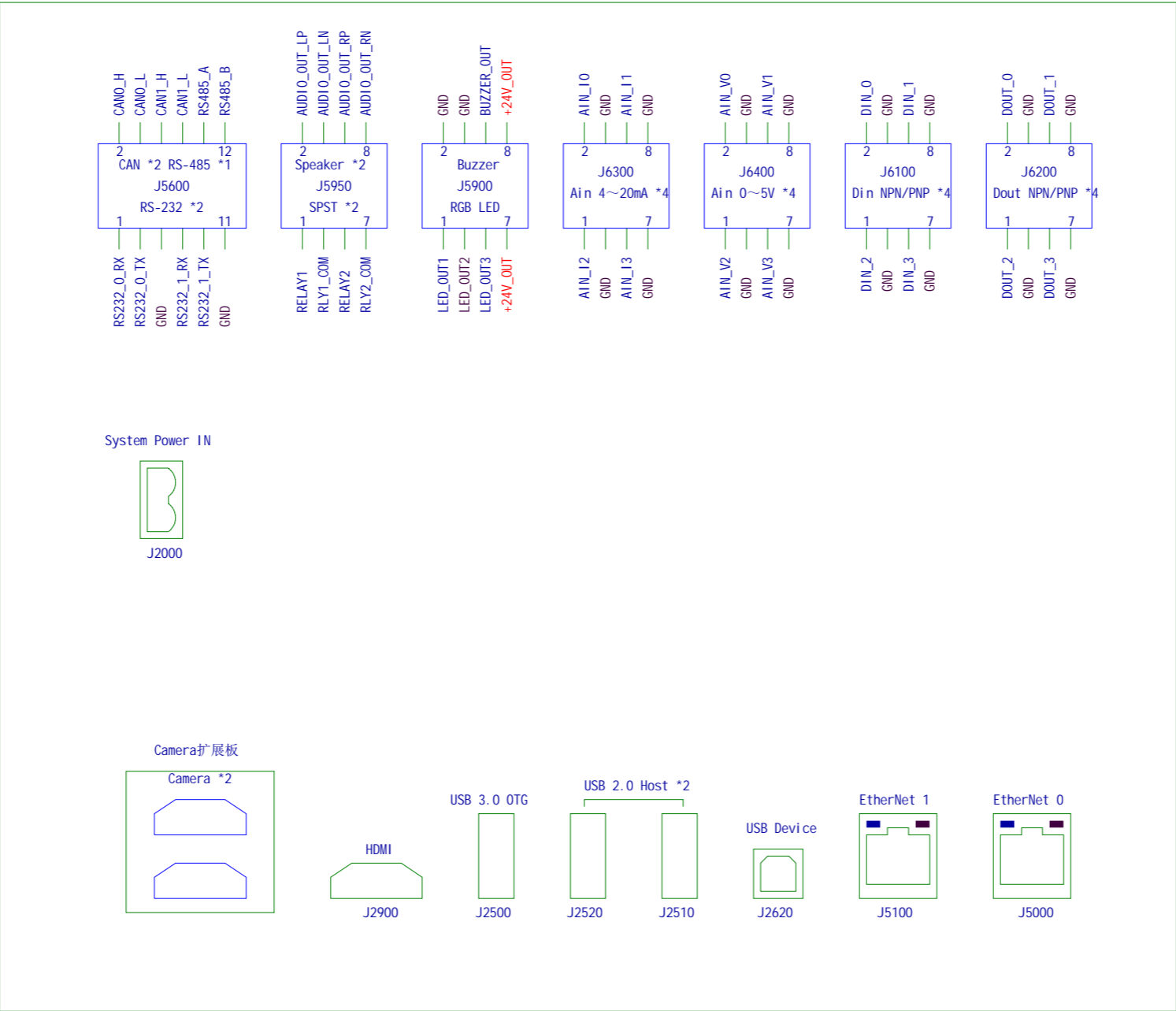
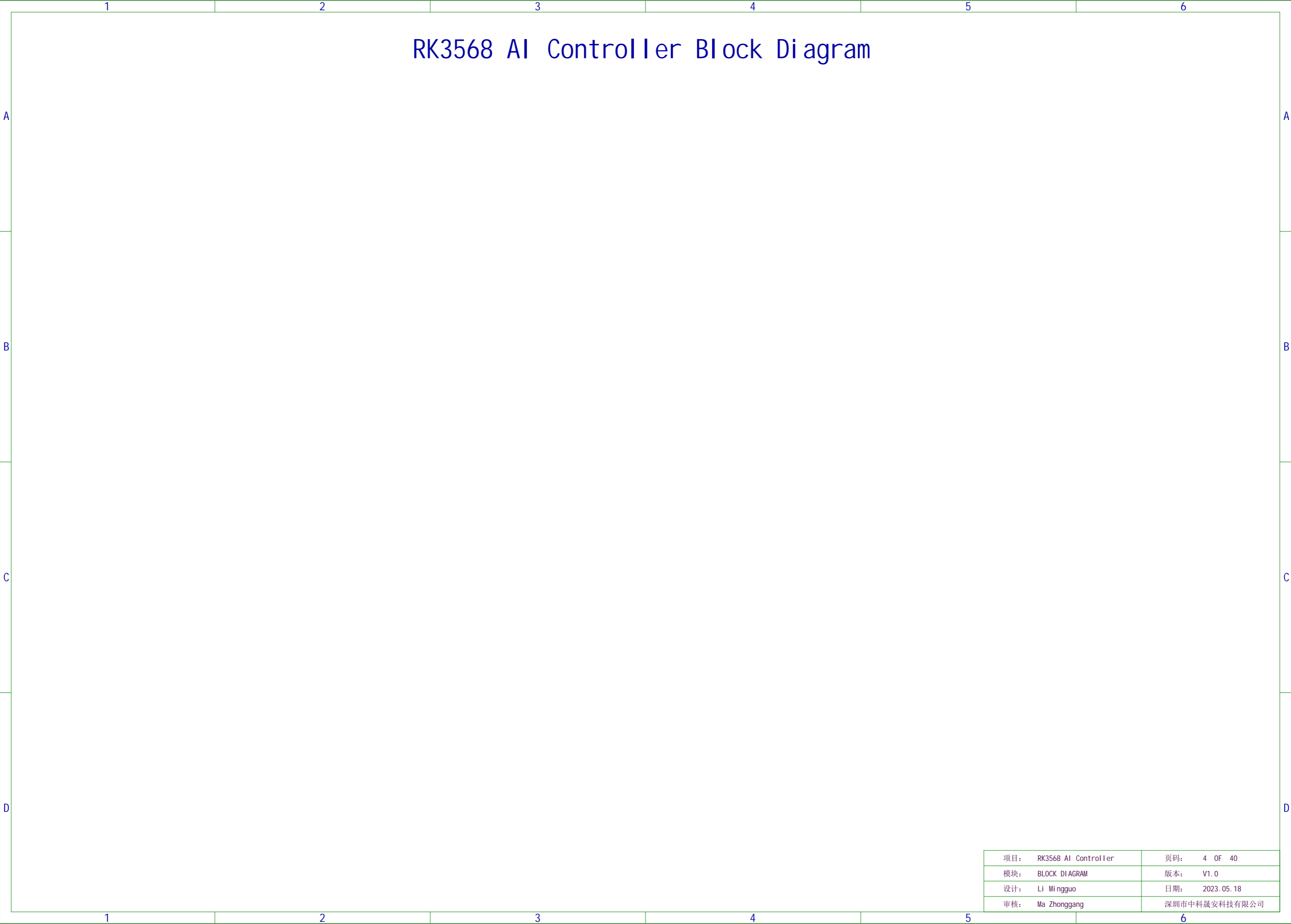


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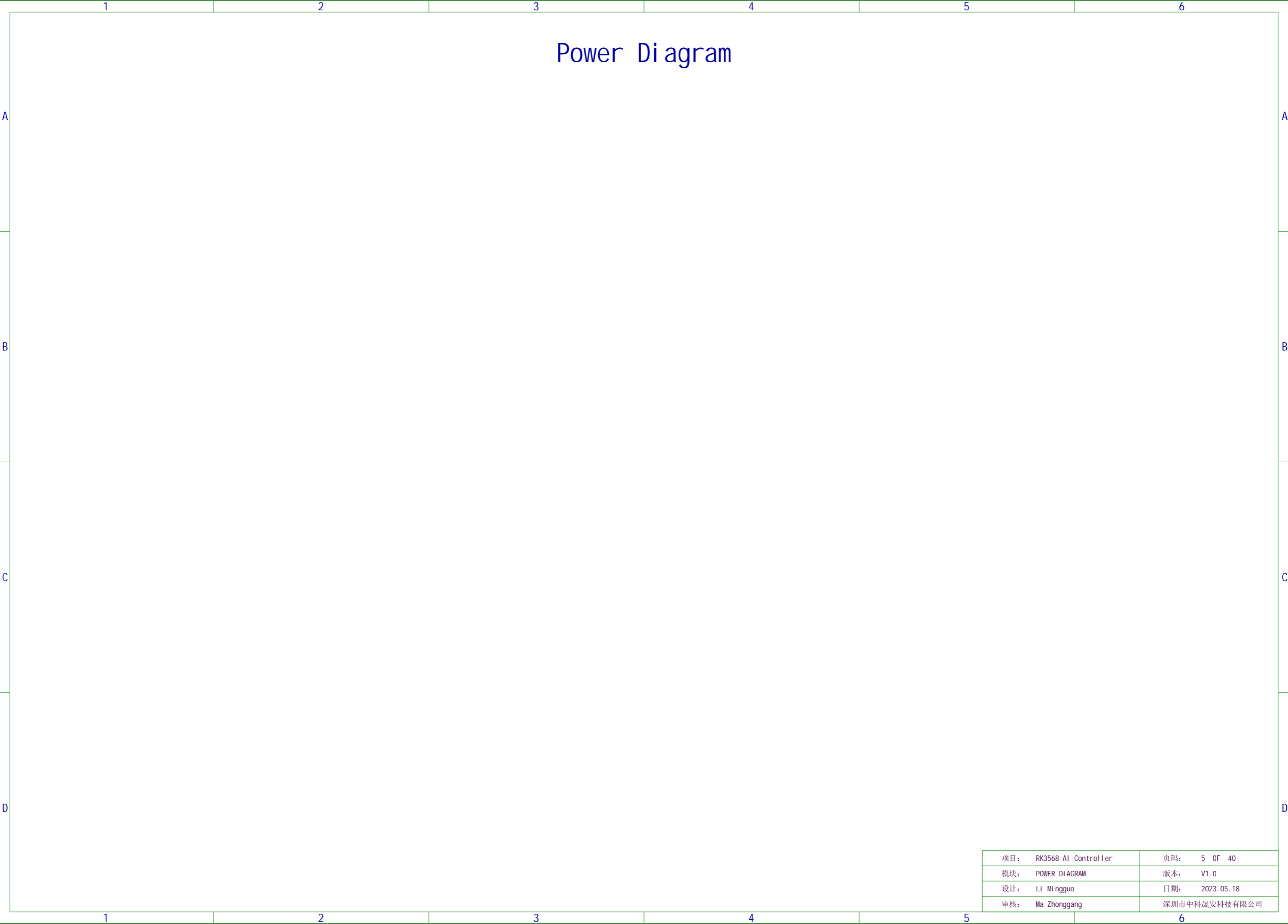
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RK3568 AI Controller Panel Diagram





项目:	RK3568 AI Controller	页码:	4 OF 40
模块:	BLOCK DIAGRAM	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang	深圳市中科晟安科技有限公司	

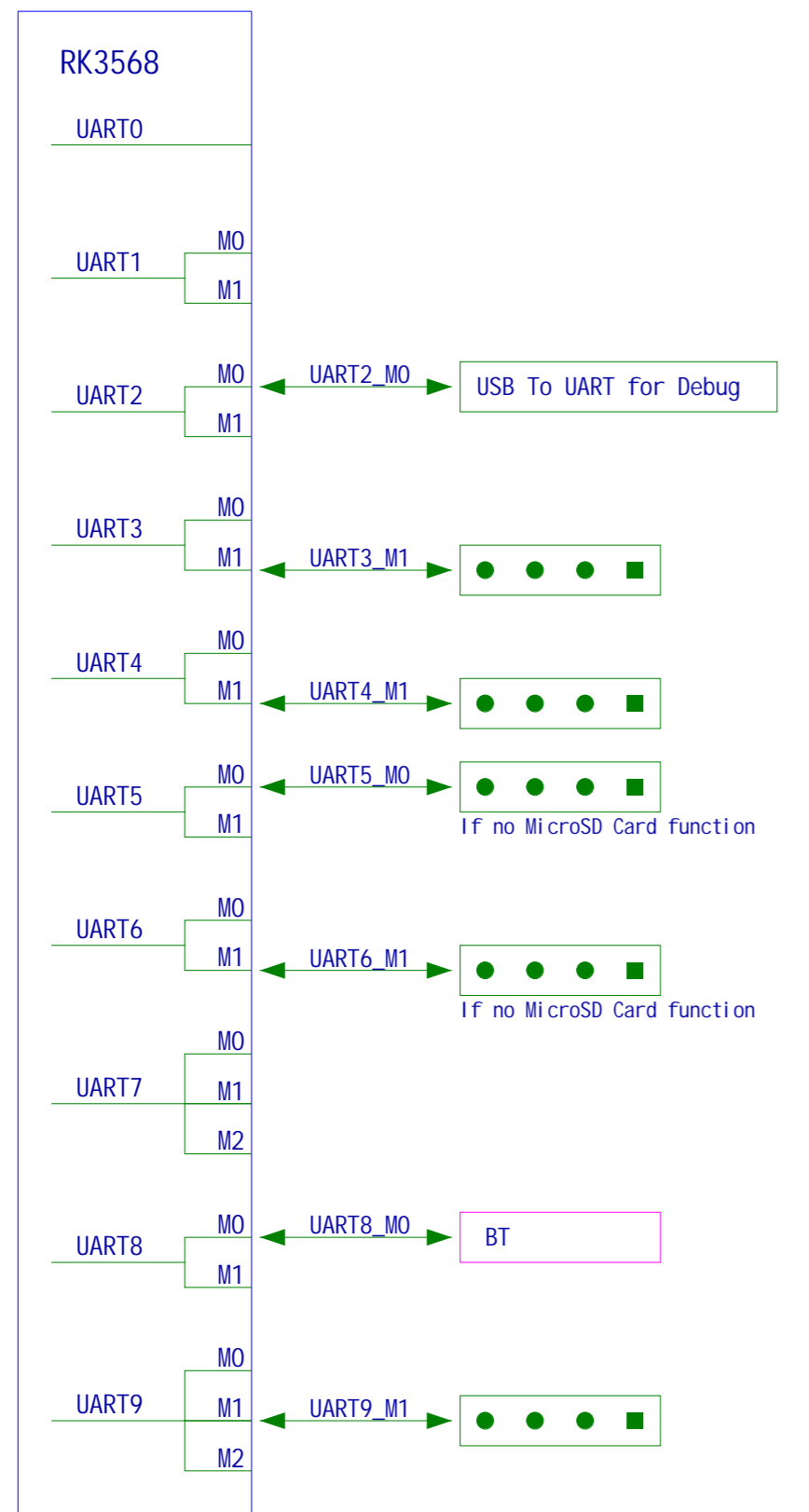


Power Diagram

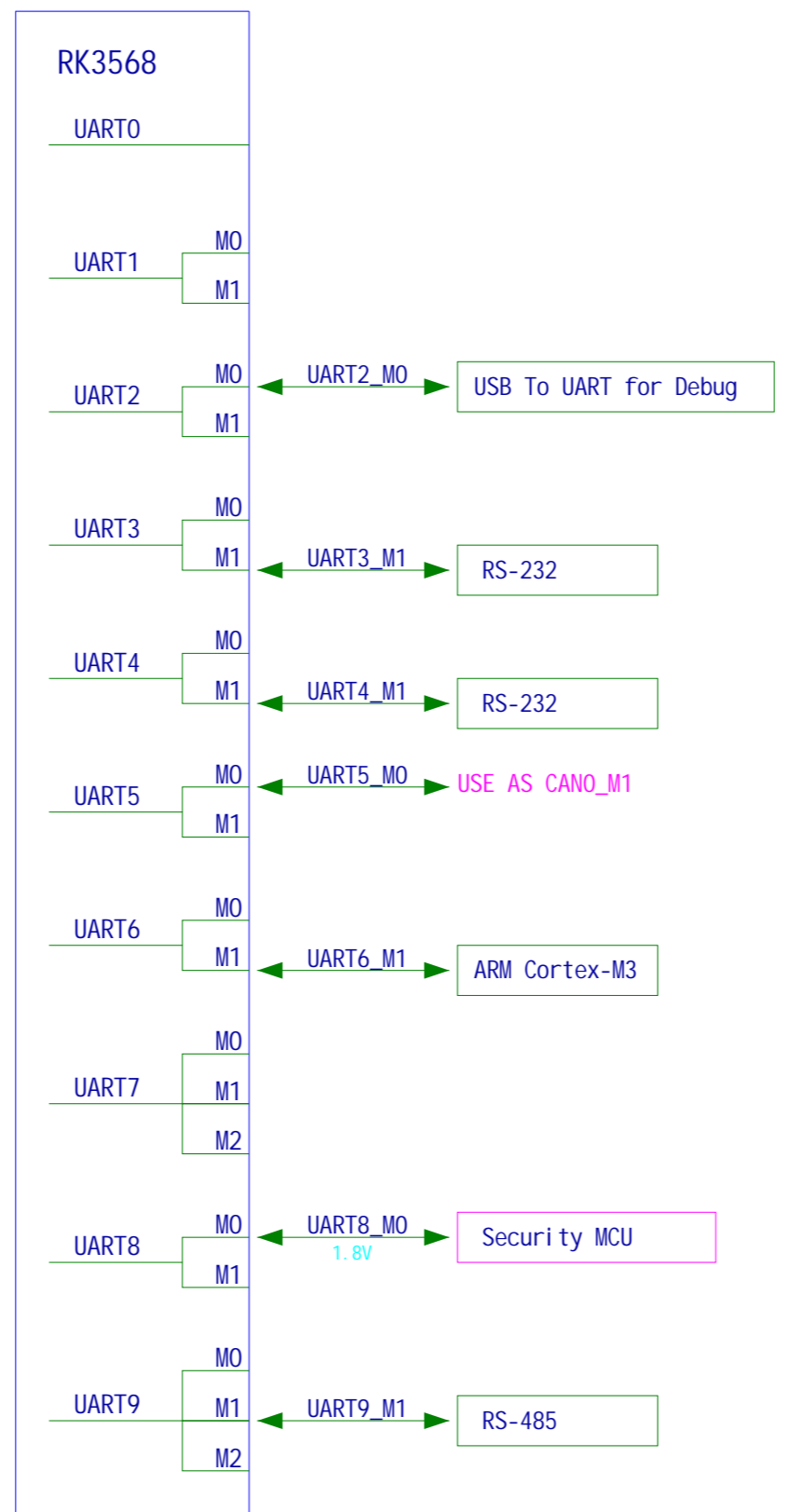
项目:	RK3568 AI Controller	页码:	5 OF 40
模块:	POWER DIAGRAM	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang	深圳市中科晟安科技有限公司	

UART MAP and CAN MAP

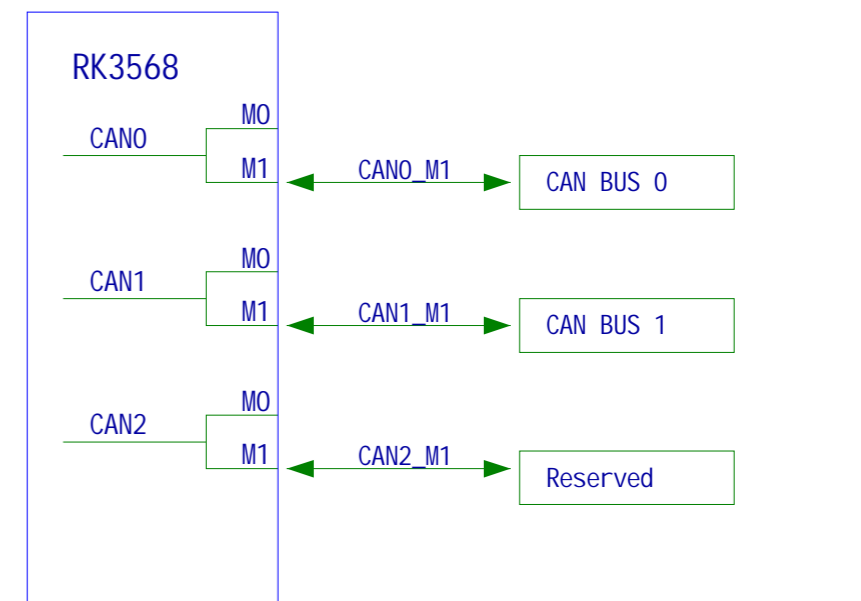
EVB UART MAP



RK3568 AI Controller UART MAP

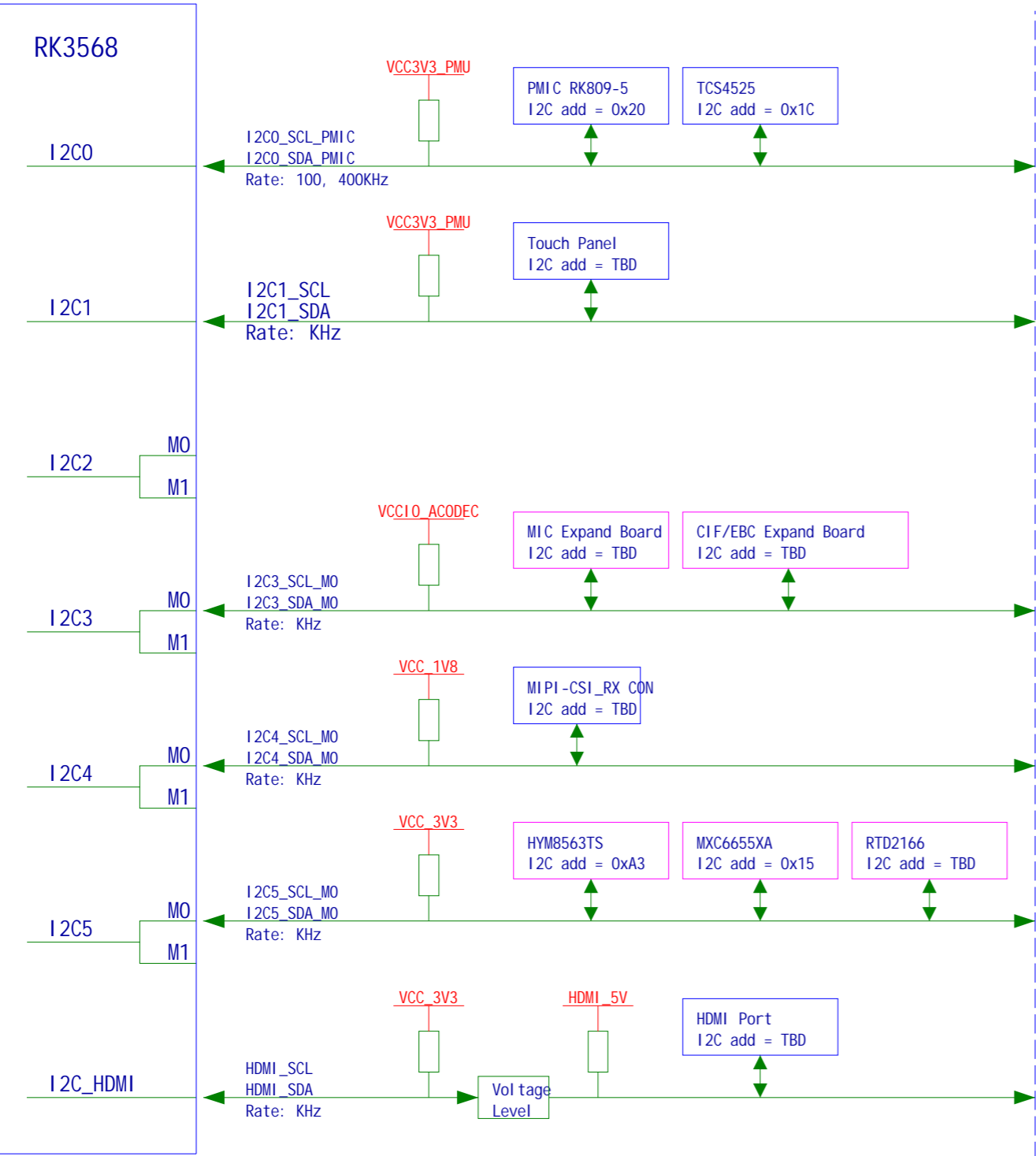


RK3568 AI Controller CAN MAP

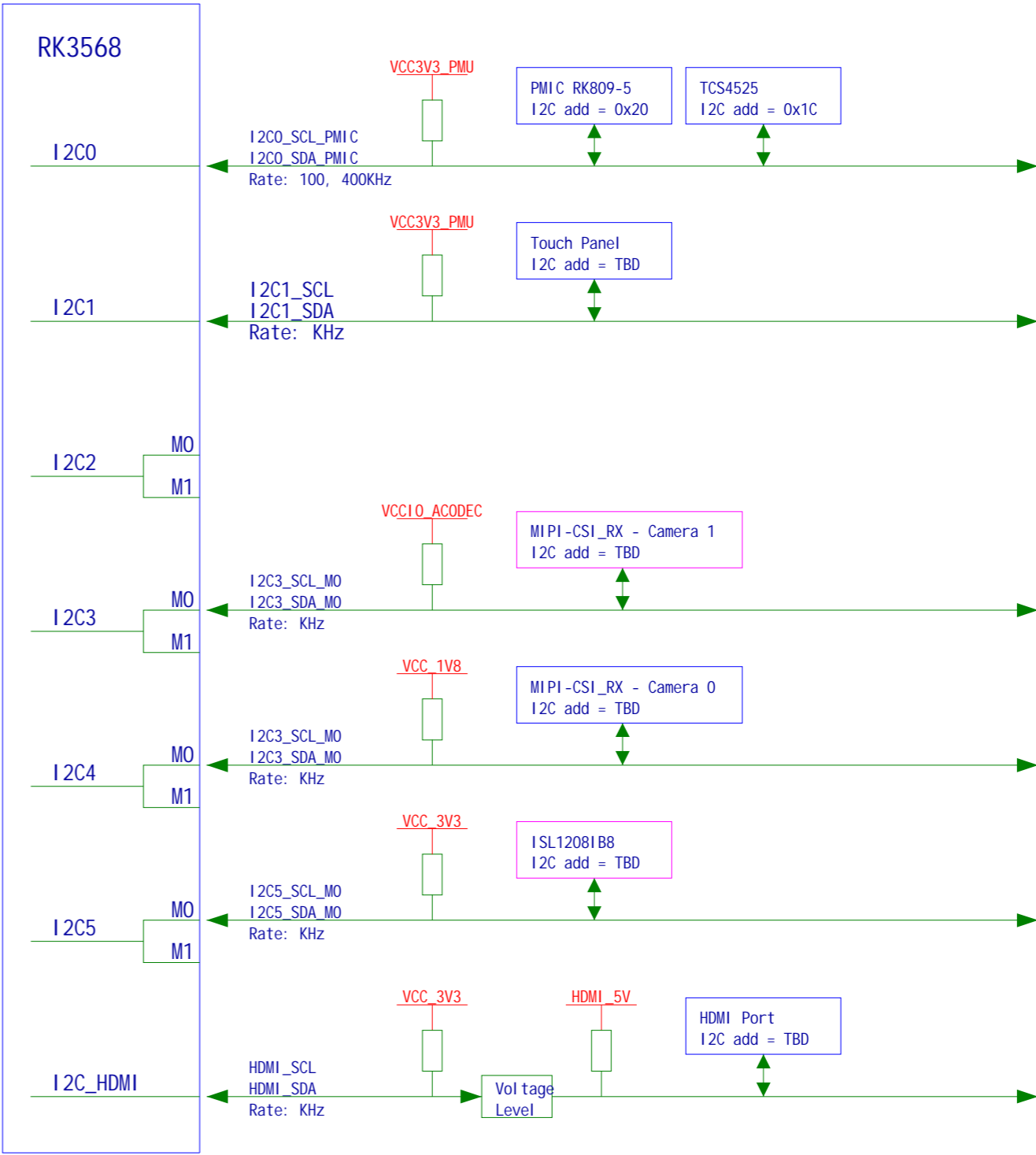


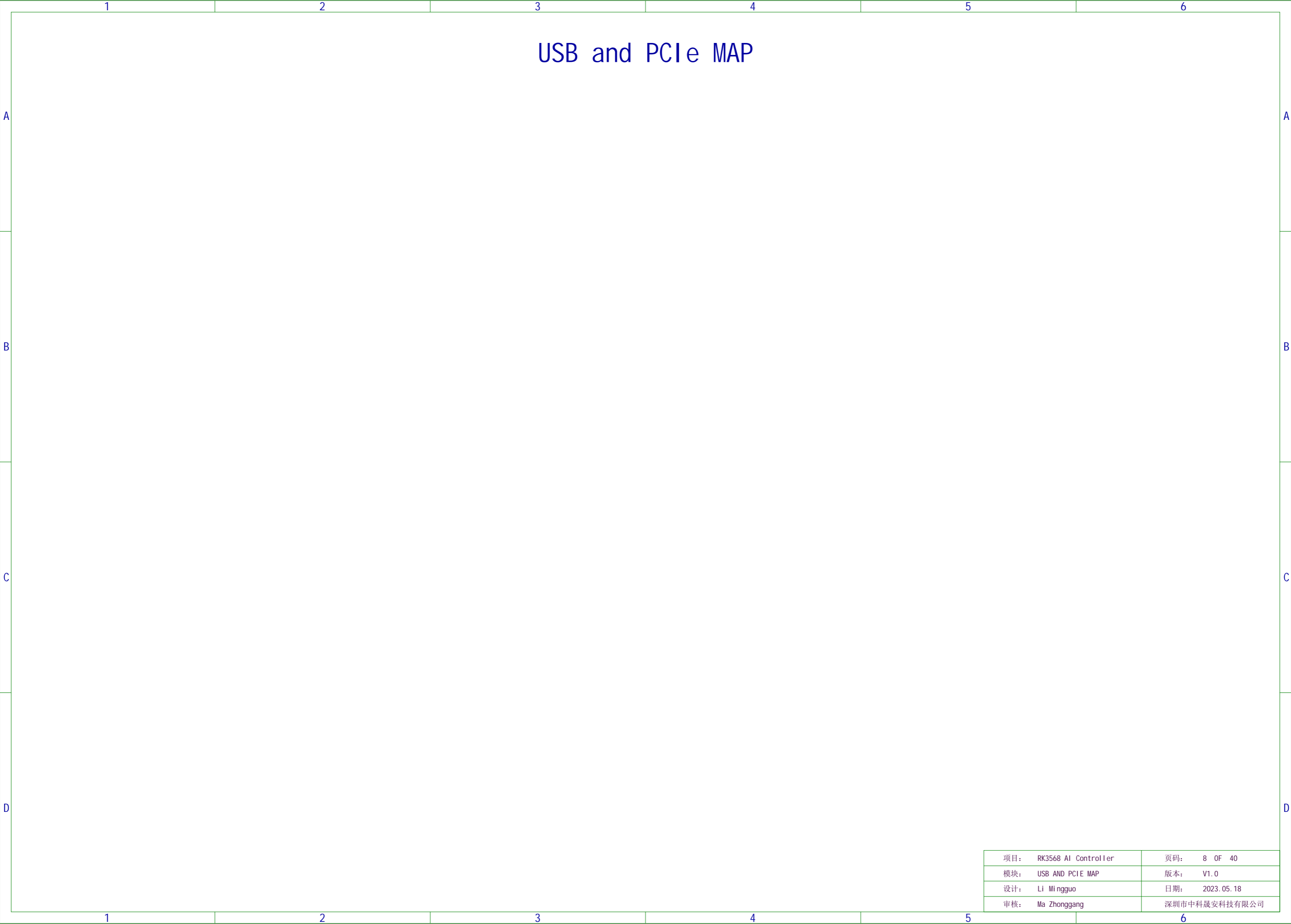
I2C MAP

EVB I2C MAP



RK3568 AI Controller I2C MAP





GPI0 Change

EVB1_RK3568 可重新分配IO

WIFI/BT	N32_RESET_L_GPI03_C6	AC5	1.8V	>>	RK3568_M, GPI03_C6, VCC106, 1.8V	EVB For SDMMC2_D0_MO	Security MCU Reset
	ARM_M3_RESET_L_GPI03_C7	AA6	1.8V	<<	RK3568_M, GPI03_C7, VCC106, 1.8V	EVB For SDMMC2_D1_MO	ARM Cortex-M3 Reset
	4G_CFG0_GPI03_D0	AB5	1.8V	<<	RK3568_M, GPI03_D0, VCC106, 1.8V	EVB For SDMMC2_D2_MO	M.2 4G/5G Module CFG[0:3]
	4G_CFG1_GPI03_D1	AB1	1.8V	<<	RK3568_M, GPI03_D1, VCC106, 1.8V	EVB For SDMMC2_D3_MO	
	4G_CFG2_GPI03_D2	Y7	1.8V	<<	RK3568_M, GPI03_D2, VCC106, 1.8V	EVB For SDMMC2_CMD_MO	Relay*2
	4G_CFG3_GPI03_D3	AC1	1.8V	<<	RK3568_M, GPI03_D3, VCC106, 1.8V	EVB For SDMMC2_CLK_MO	
	RELAY1_L_GPI03_D4	AA1	1.8V	<<	RK3568_M, GPI03_D4, VCC106, 1.8V	EVB For WIFI_WAKE_HOST_H_GPI03_D4	CAN2_M1, Reserved
	RELAY2_L_GPI03_D5	AA5	1.8V	<<	RK3568_M, GPI03_D5, VCC106, 1.8V	EVB For WIFI_REG_ON_H_GPI03_D5	
	CAN2_RX_M1	D26	1.8V	<<	RK3568_K, GPI02_B1, VCC104, 1.8V	EVB For UART8_RTSn_MO	Security MCU UART
	CAN2_TX_M1	E25	1.8V	<<	RK3568_K, GPI02_B2, VCC104, 1.8V	EVB For UART8_CTSn_MO	
	UART8_TX_MO	F26	1.8V	>>	RK3568_K, GPI02_C5, VCC104, 1.8V	EVB For WIFI/BT	M.2 4G/5G Module
	UART8_RX_MO	E26	1.8V	<<	RK3568_K, GPI02_C6, VCC104, 1.8V		
	4G_POWER_EN_L_GPI03_A0	AH4	3.3V	>>	RK3568_L, GPI03_A0, VCC105, 3.3V	EVB For BT_REG_ON_H_GPI03_A0	RK Din *4 Channels
	4G_POWER_KEY_L_GPI03_A1	AB8	3.3V	>>	RK3568_L, GPI03_A1, VCC105, 3.3V	EVB For BT_WAKE_HOST_H_GPI03_A1	
	4G_RESET_L_GPI03_A2	AE5	3.3V	>>	RK3568_L, GPI03_A2, VCC105, 3.3V	EVB For HOST_WAKE_BT_H_GPI03_A2	
	RK_DIN_0_GPI03_A3	AG4	3.3V	<<	RK3568_L, GPI03_A3, VCC105, 3.3V	EVB For I2S3_SCLK_MO	
	RK_DIN_1_GPI03_A4	AF4	3.3V	<<	RK3568_L, GPI03_A4, VCC105, 3.3V	EVB For I2S3_LRCK_MO	
	RK_DIN_2_GPI03_A5	AH3	3.3V	<<	RK3568_L, GPI03_A5, VCC105, 3.3V	EVB For I2S3_SDO_MO	
	RK_DIN_3_GPI03_A6	AG3	3.3V	<<	RK3568_L, GPI03_A6, VCC105, 3.3V	EVB For I2S3_SDI_MO	

RK3568_L	RK_DIN_CTRL_GPI03_C1	AD1	3.3V	>>	RK3568_L, GPI03_C1, VCC105, 3.3V	EVB For SENSOR_INT_L_GPI03_C1	RK Din *4 Channels
	AUDIO_PA_FAULT_L_GPI03_C2	AA7	3.3V	<<	RK3568_L, GPI03_C2, VCC105, 3.3V	EVB For HP_DET_L_GPI03_C2	Audio Power Amplifier
	AUDIO_PA_SD_H_GPI03_C3	AC4	3.3V	<<	RK3568_L, GPI03_C3, VCC105, 3.3V	EVB For PA_EN_H_GPI03_C3	

PWM	LED_OUT1_PWM3_IR	AG23	3.3V	>>	RK3568_G, GPI00_C2, PMU102, 3.3V	EVB For DP_HPDI_N_M1	PWM for LED*3 and Buzzer
	LED_OUT2_PWM5	AD21	3.3V	>>	RK3568_G, GPI00_C4, PMU102, 3.3V	EVB For LCD1_BL_PWM5	
	LED_OUT3_PWM7_IR	AD20	3.3V	>>	RK3568_G, GPI00_C6, PMU102, 3.3V	EVB For PWM7_IR	
	BUZZER_PWM15_IR_MO	AC2	3.3V	>>	RK3568_L, GPI03_C5, VCC105, 3.3V	EVB For Audio-S/PDIF_TX_Port	

RK3568_G	RK_DOUT_0_GPI00_A4	Y22	3.3V	>>	RK3568_G, GPI00_A4, PMU101, 3.3V	EVB For SDMMC0_DET_L	RK Dout *4 Channels
	RK_DOUT_1_GPI00_B0	AD23	3.3V	>>	RK3568_G, GPI00_B0, PMU102, 3.3V	EVB For CLK32K_OUT0_WIFI	
	LCD0_RST_L_GPI00_C5	AC21	3.3V	>>	RK3568_G, GPI00_C5, PMU102, 3.3V	EVB For LCD1_PWREN_H_GPI00_C5	LCD0 RESET
	RK_DOUT_CTRL_GPI00_D5	AD25	1.8V	>>	RK3568_G, GPI00_D5, PMUPLL_AVDD_1V8, 1.8V	EVB For VGA_PWREN_H_GPI00_D5	RK Dout *4 Channels
	CPU_AVS/CPU_DVS_PWM0_MO	AH26	3.3V		RK3568_G, GPI00_B7, PMU102, 3.3V	NC, VDD_CPU_EXT	
	GPI00_D3	AE26	1.8V		RK3568_G, GPI00_D3, PMUPLL_AVDD_1V8, 1.8V	NC, RTC_INT	
	GPI00_D6	AC24	1.8V		RK3568_G, GPI00_D6, PMUPLL_AVDD_1V8, 1.8V	NC, TP	

RK3568_N	RK_DOUT_2_GPI04_C4	AH7	3.3V		RK3568_N, GPI04_C4, VCC107, 3.3V	EVB for SATA2_ACT_LED	RK Dout *4 Channels
	RS485_TX_EN_L_GPI04_D2	AB9	3.3V		RK3568_N, GPI04_D2, VCC107, 3.3V	EVB CON_INT_L_GPI04_D2	RS-485_DIR

RK3568_H	I2C3_SDA_MO	D18	3.3V	<<	RK3568_H, GPI01_A0, VCC101, 3.3V	EVB: Audio Extended Board	Camera: MIPI-CSI
	I2C3_SCL_MO	E18	3.3V	>>	RK3568_H, GPI01_A1, VCC101, 3.3V		RK Dout *4 Channels
	RK_DOUT_3_GPI01_A4	F18	3.3V	>>	RK3568_H, GPI01_A4, VCC101, 3.3V	EVB: I2S1_SCLK_RX_MO/PDM_CLK1_MO	

RK3568 AI Controller IO 分配

Audio Power Amplifier

Din *4 Channels (NPN/PNP)

To RK3568, Optional

Dout *4 Channels (NPN/PNP)

From RK3568, Optional

M.2 4G/5G Module CFG[0:3]

M.2 4G/5G Module Control

RS-485

Dout for LED*3 and Buzzer

Relay*2

ARM Cortex-M3

Security MCU

Camera: MIPI-CSI

<<	AUDIO_PA_FAULT_L_GPI03_C2	AA7	3.3V	<<	RK3568_L, GPI03_C2, VCC105, 3.3V	EVB For HP_DET_L_GPI03_C2
>>	AUDIO_PA_SD_H_GPI03_C3	AC4	3.3V	>>	RK3568_L, GPI03_C3, VCC105, 3.3V	EVB For PA_EN_H_GPI03_C3

>>	RK_DIN_CTRL_GPI03_C1	AD1	3.3V	>>	RK3568_L, GPI03_C1, VCC105, 3.3V	EVB For SENSOR_INT_L_GPI03_C1
<<	RK_DIN_0_GPI03_A3	AG4	3.3V	<<	RK3568_L, GPI03_A3, VCC105, 3.3V	EVB For I2S3_SCLK_MO
<<	RK_DIN_1_GPI03_A4	AF4	3.3V	<<	RK3568_L, GPI03_A4, VCC105, 3.3V	EVB For I2S3_LRCK_MO
<<	RK_DIN_2_GPI03_A5	AH3	3.3V	<<	RK3568_L, GPI03_A5, VCC105, 3.3V	EVB For I2S3_SDO_MO
<<	RK_DIN_3_GPI03_A6	AG3	3.3V	<<	RK3568_L, GPI03_A6, VCC105, 3.3V	EVB For I2S3_SDI_MO

>>	RK_DOUT_CTRL_GPI00_D5	AD25	1.8V	>>	RK3568_G, GPI00_D5, PMUPLL_AVDD_1V8, 1.8V	EVB For VGA_PWREN_H_GPI00_D5	VO-VGA out
>>	RK_DOUT_0_GPI00_A4	Y22	3.3V	>>	RK3568_G, GPI00_A4, PMU101, 3.3V	EVB For SDMMC0_DET_L	For MicroSD Card
>>	RK_DOUT_1_GPI00_B0	AD23	3.3V	>>	RK3568_G, GPI00_B0, PMU102, 3.3V	EVB For CLK32K_OUT0_WIFI	For WIFI/BT
>>	RK_DOUT_2_GPI04_C4	AH7	3.3V	>>	RK3568_N, GPI04_C4, VCC107, 3.3V	EVB For SATA2_ACT_LED	
>>	RK_DOUT_3_GPI01_A4	F18	3.3V	>>	RK3568_H, GPI01_A4, VCC101, 3.3V	EVB For I2S1_SCLK_RX_MO/PDM_CLK1_MO	Audio Extended Board

<<	4G_CFG0_GPI03_D0	AB5	1.8V	<<	RK3568_M, GPI03_D0, VCC106, 1.8V	EVB For SDMMC2_D2_MO
<<	4G_CFG1_GPI03_D1	AB1	1.8V	<<	RK3568_M, GPI03_D1, VCC106, 1.8V	EVB For SDMMC2_D3_MO
<<	4G_CFG2_GPI03_D2	Y7	1.8V	<<	RK3568_M, GPI03_D2, VCC106, 1.8V	EVB For SDMMC2_CMD_MO
<<	4G_CFG3_GPI03_D3	AC1	1.8V	<<	RK3568_M, GPI03_D3, VCC106, 1.8V	EVB For SDMMC2_CLK_MO

>>	4G_POWER_EN_L_GPI03_A0	AH4	3.3V	>>	RK3568_L, GPI03_A0, VCC105, 3.3V	EVB For BT_REG_ON_H_GPI03_A0
>>	4G_POWER_KEY_L_GPI03_A1	AB8	3.3V	>>	RK3568_L, GPI03_A1, VCC105, 3.3V	EVB For BT_WAKE_HOST_H_GPI03_A1
>>	4G_RESET_L_GPI03_A2	AE5	3.3V	>>	RK3568_L, GPI03_A2, VCC105, 3.3V	EVB For HOST_WAKE_BT_H_GPI03_A2

RS-485_DIR	>>	RS485_TX_EN_L_GPI04_D2	AB9	3.3V	RK3568_N, GPI04_D2, VCC107, 3.3V	EVB For CON_INT_L_GPI04_D2
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LED_OUT *3	>>	LED_OUT1_PWM3_IR	AG23	3.3V	RK3568_G, GPI00_C2, PMU102, 3.3V	EVB For DP_HPDI_N_M1
	>>	LED_OUT2_PWM5	AD21	3.3V	RK3568_G, GPI00_C4, PMU102, 3.3V	EVB For LCD1_BL_PWM5
	>>	LED_OUT3_PWM7_IR	AD20	3.3V	RK3568_G, GPI00_C6, PMU102, 3.3V	EVB For PWM7_IR
Buzzer	>>	BUZZER_PWM15_IR_MO	AC2	3.3V	RK3568_L, GPI03_C5, VCC105, 3.3V	EVB For Audio-S/PDIF_TX_Port

Relay*2	>>	RELAY1_L_GPI03_D4	AA1	1.8V	RK3568_M, GPI03_D4, VCC106, 1.8V	EVB For WIFI_WAKE_HOST_H_GPI03_D4
	>>	RELAY2_L_GPI03_D5	AA5	1.8V	RK3568_M, GPI03_D5, VCC106, 1.8V	EVB For WIFI_REG_ON_H_GPI03_D5

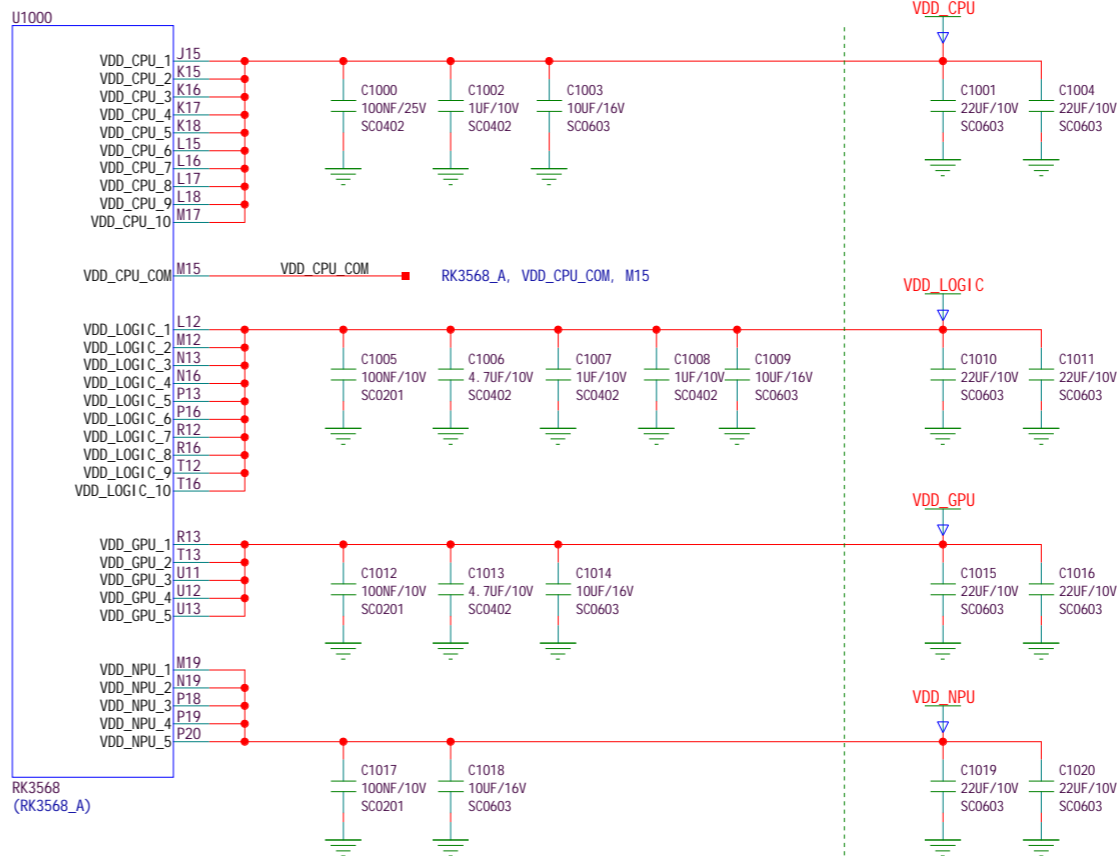
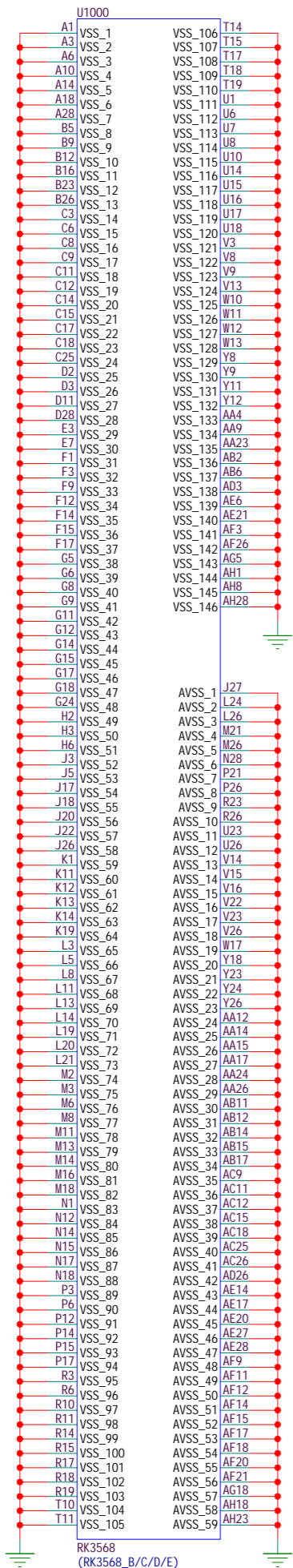
>>	ARM_M3_RESET_L_GPI03_C7	AA6	1.8V	>>	RK3568_M, GPI03_C7, VCC106, 1.8V	EVB For SDMMC2_D1_MO
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Security MCU Reset, NC	>>	N32_RESET_L_GPI03_C6	AC5	1.8V	RK3568_M, GPI03_C6, VCC106, 1.8V	EVB For SDMMC2_D0_MO
UART8_MO	>>	UART8_TX_MO	F26	1.8V	RK3568_K, GPI02_C5, VCC104, 1.8V	EVB For WIFI/BT
	<<	UART8_RX_MO	E26	1.8V	RK3568_K, GPI02_C6, VCC104, 1.8V	

I2C3	<<	I2C3_SDA_MO	D18	3.3V	RK3568_H, GPI01_A0, VCC101, 3.3V	EVB For Audio Extended Board
	>>	I2C3_SCL_MO	E18	3.3V	RK3568_H, GPI01_A1, VCC101, 3.3V	

项目:	RK3568 AI Controller	页码:	9 OF 40
模块:	RK3568 GPIO CHANGE	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

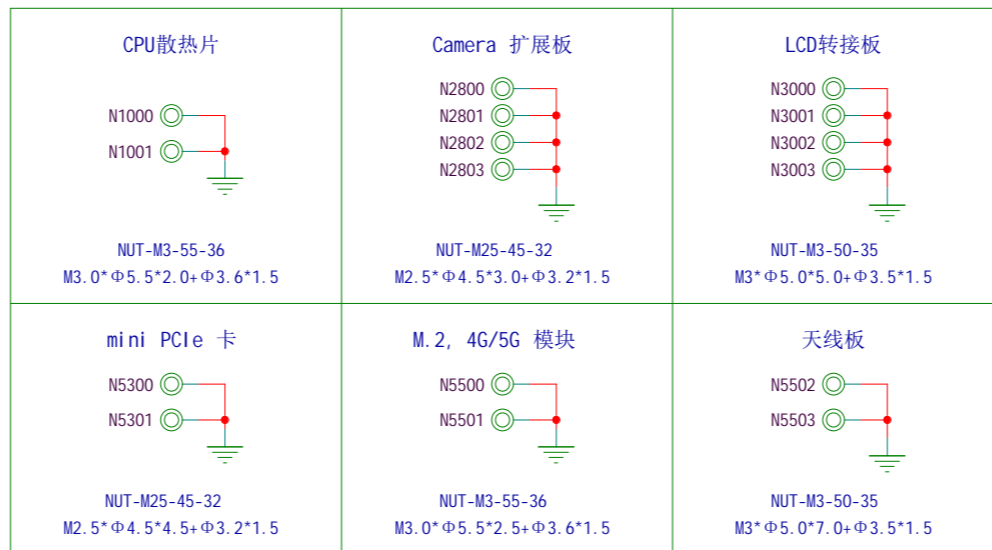
RK3568_ABCDE (Power & Gnd)



Caps should be placed under the RK3568 package

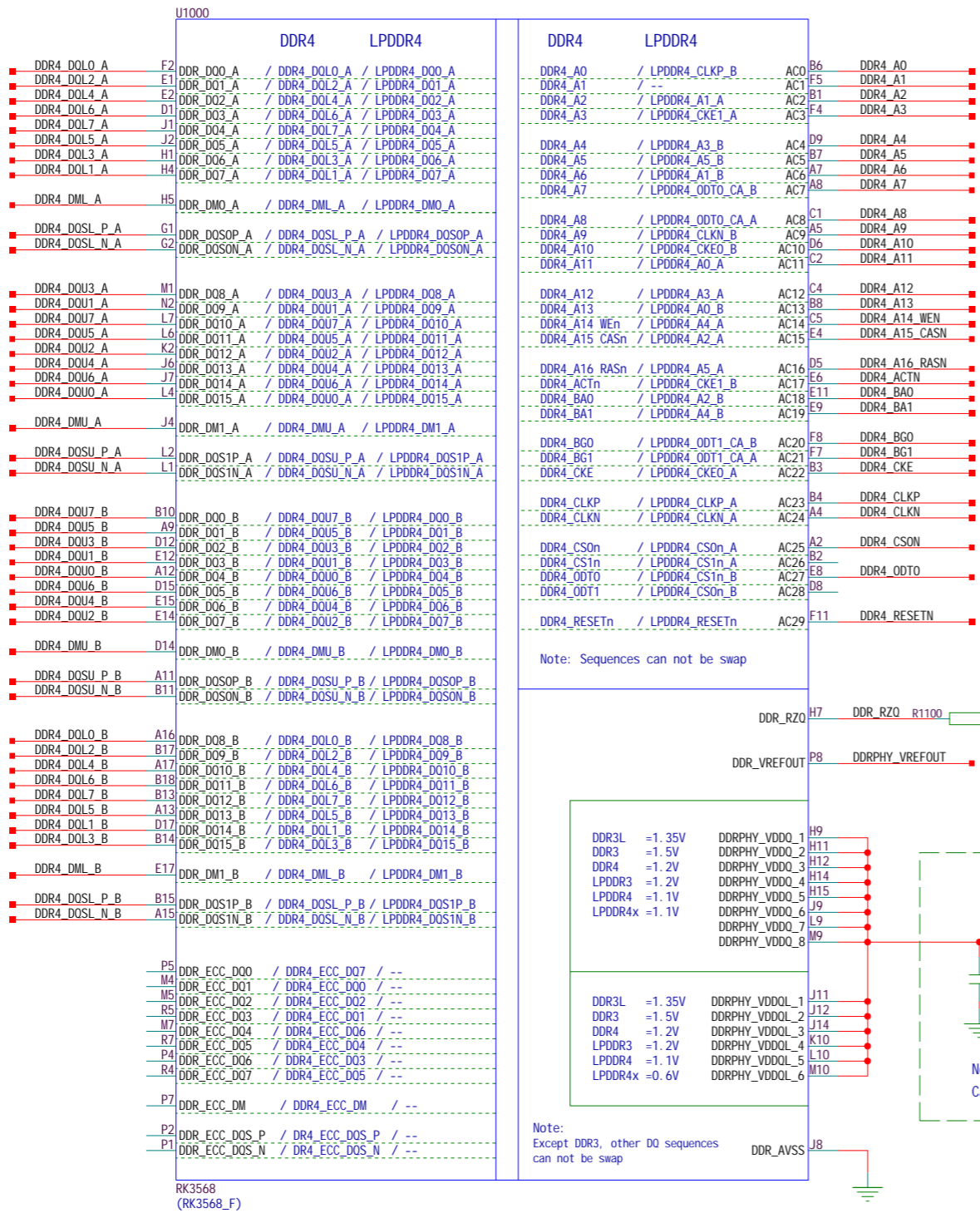
Caps should be placed close to the RK3568 package

SMT贴片铜螺母



项目:	RK3568 AI Controller	页码:	10 OF 40
模块:	RK3568_POWER/GND	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

RK3568_F (DDR PHY)



项目:	RK3568 AI Controller	页码:	11 OF 40
模块:	RK3568_DDR PHY	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

B

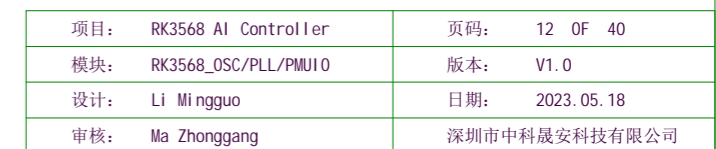
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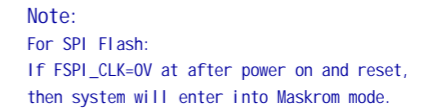
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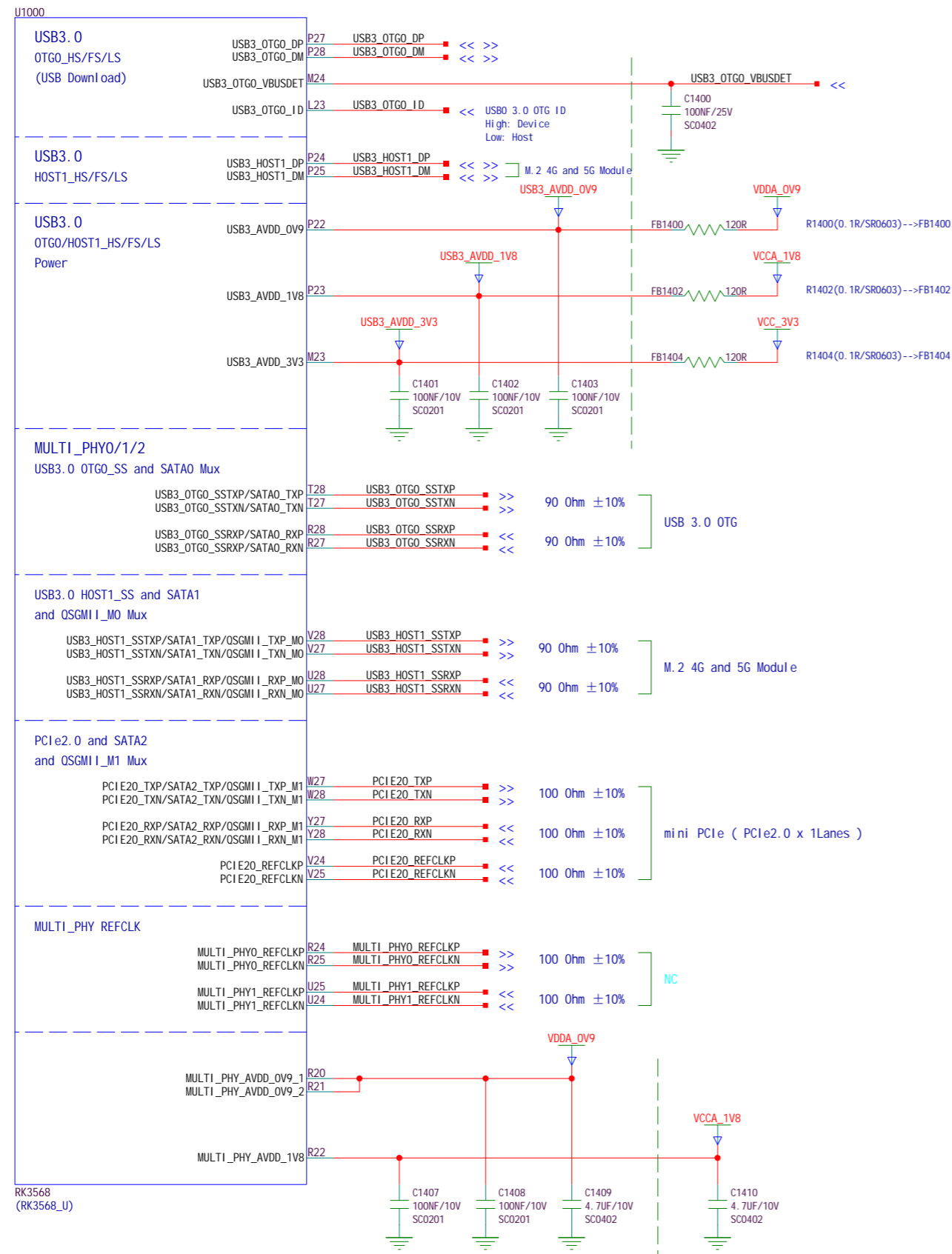
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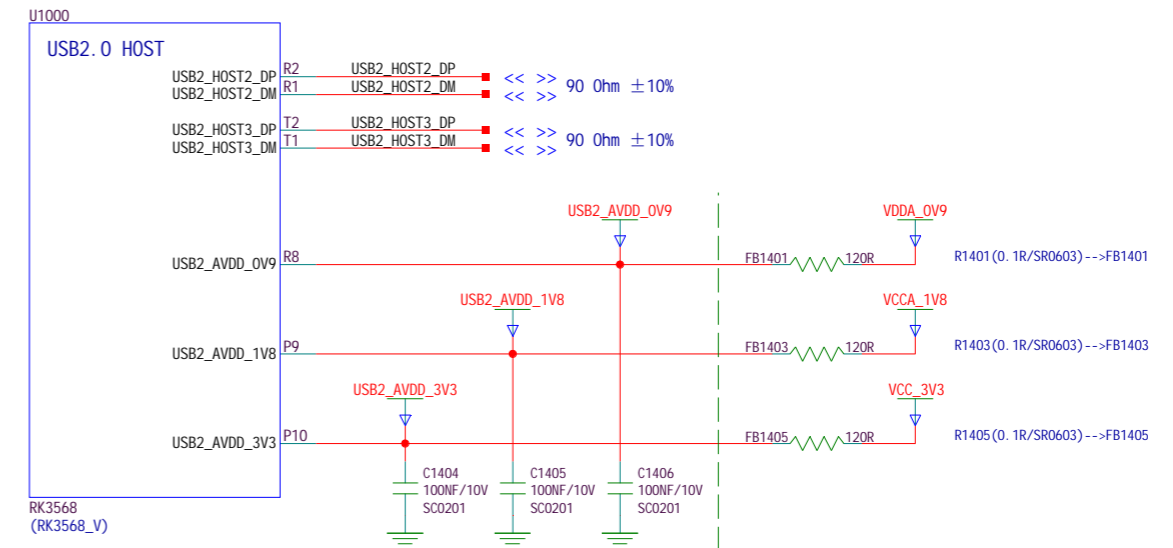
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RK3568_U (USB3.0 / SATA / QSGMI I / PCIe2.0 x1)

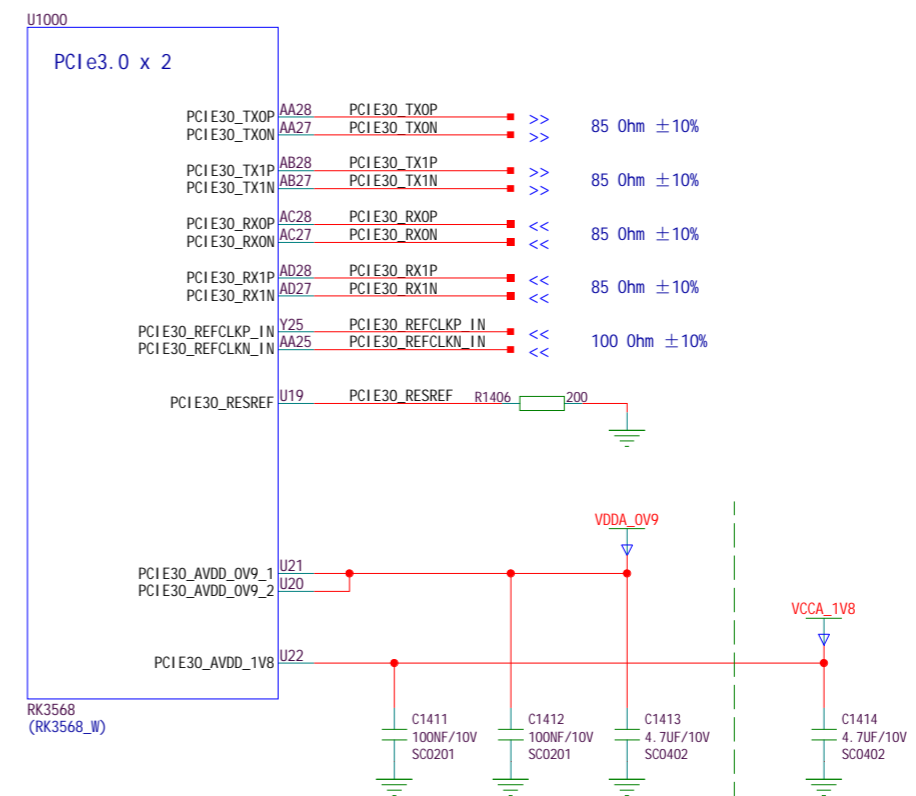


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V (USB2.0 HOST)

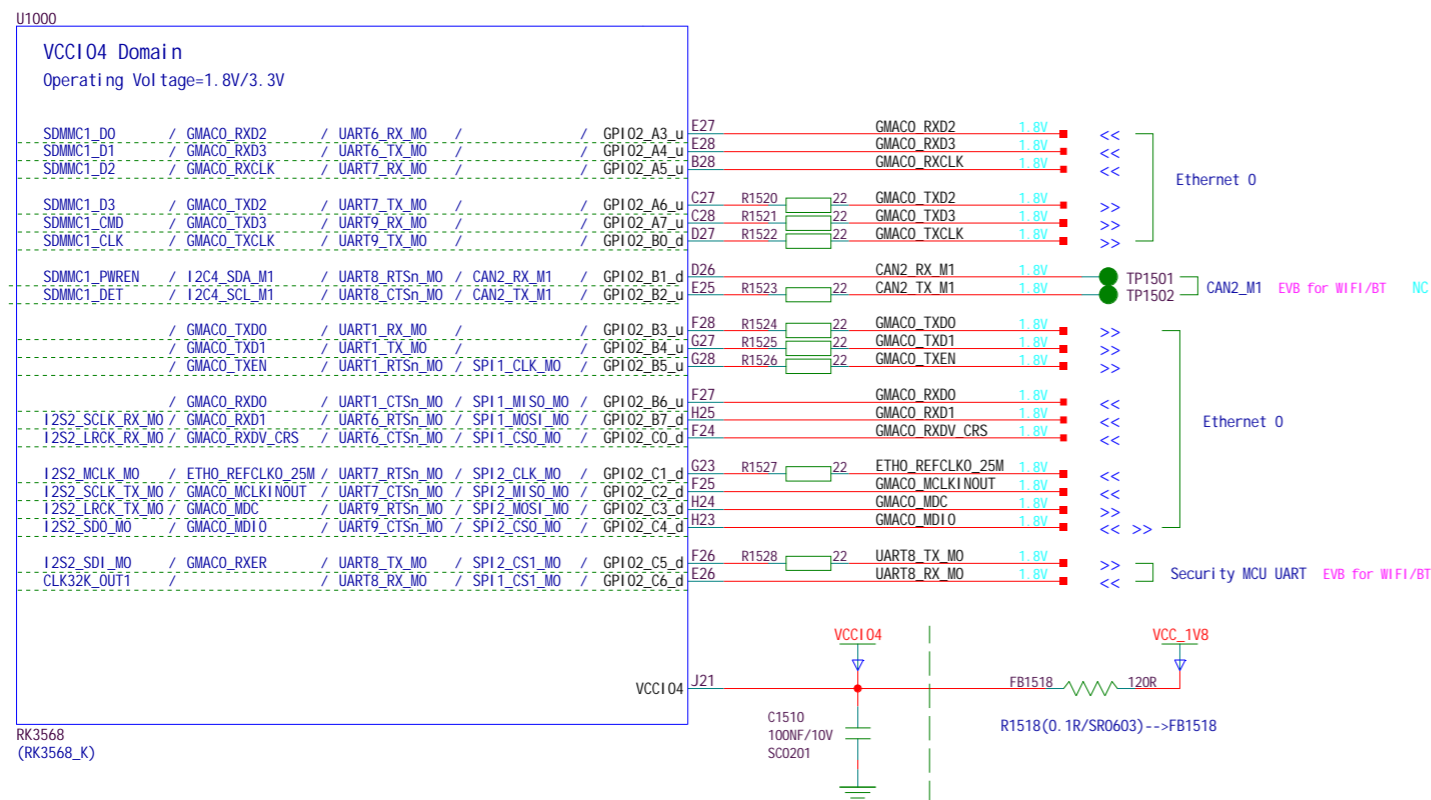


RK3568_W (PCIe3.0 x2)

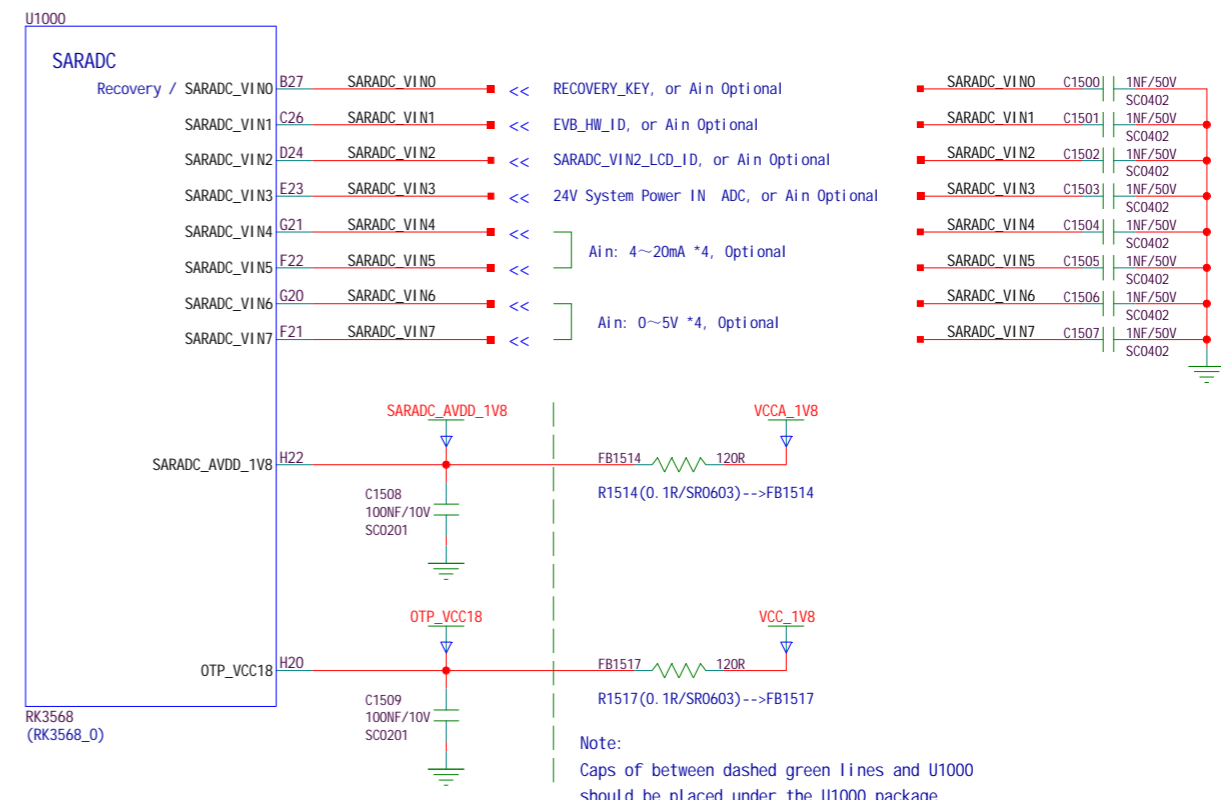


项目:	RK3568 AI Controller	页码:	14 OF 40
模块:	RK3568_USB/PCI E/SATA PHY	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

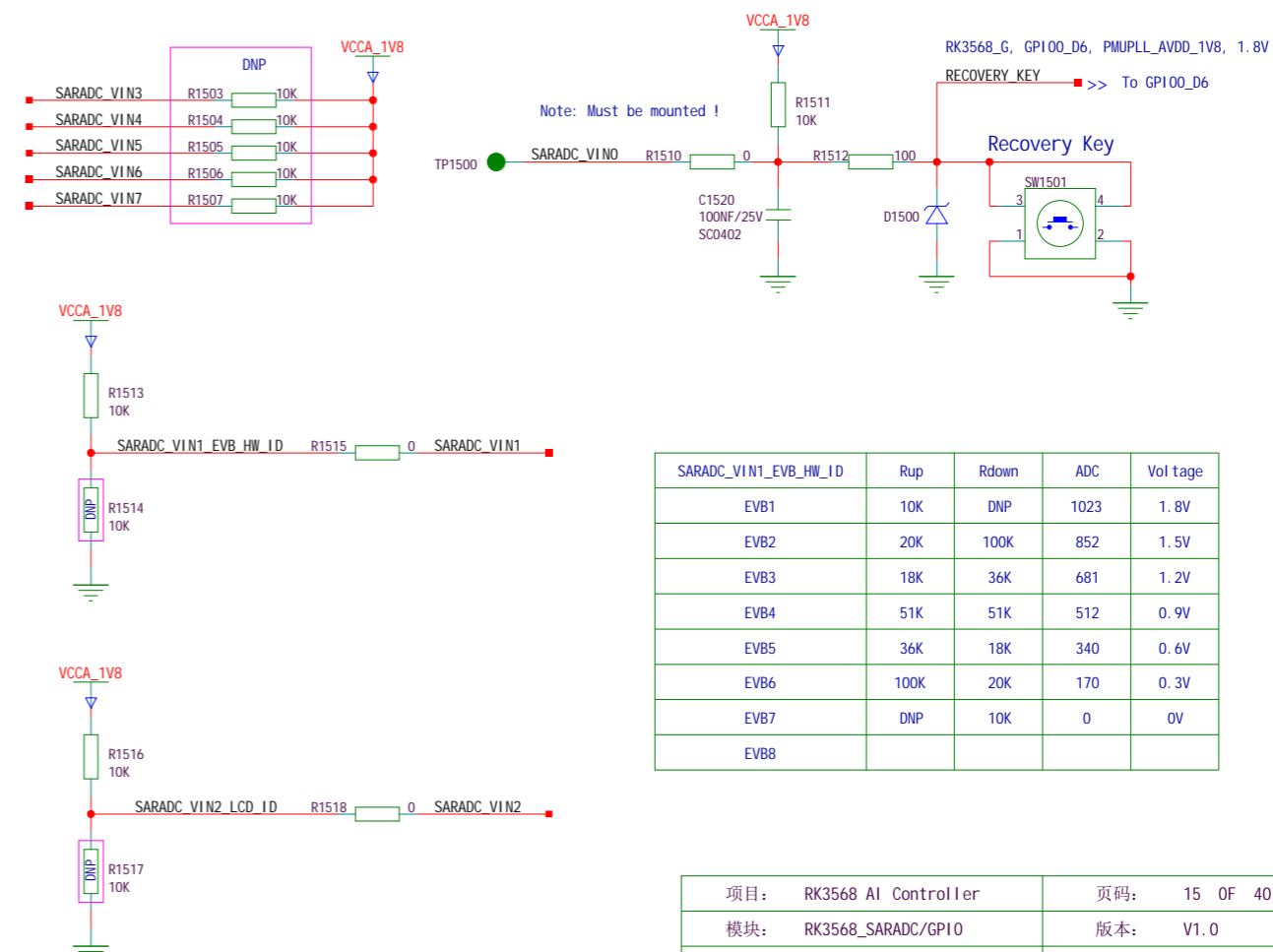
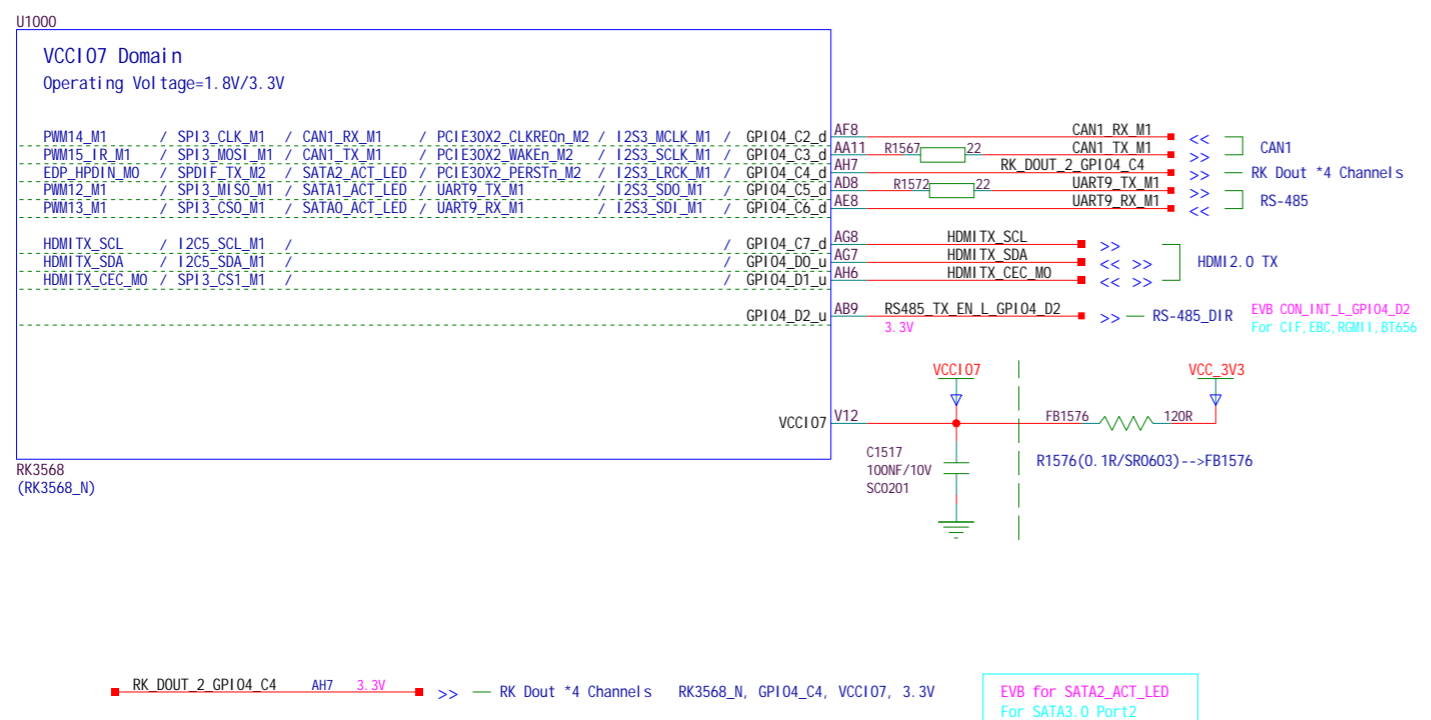
RK3568_K UART / GMACO (VCCI04 Domain)



RK3568_O (SARADC/OTP)



RK3568_N (VCCI07 Domain)

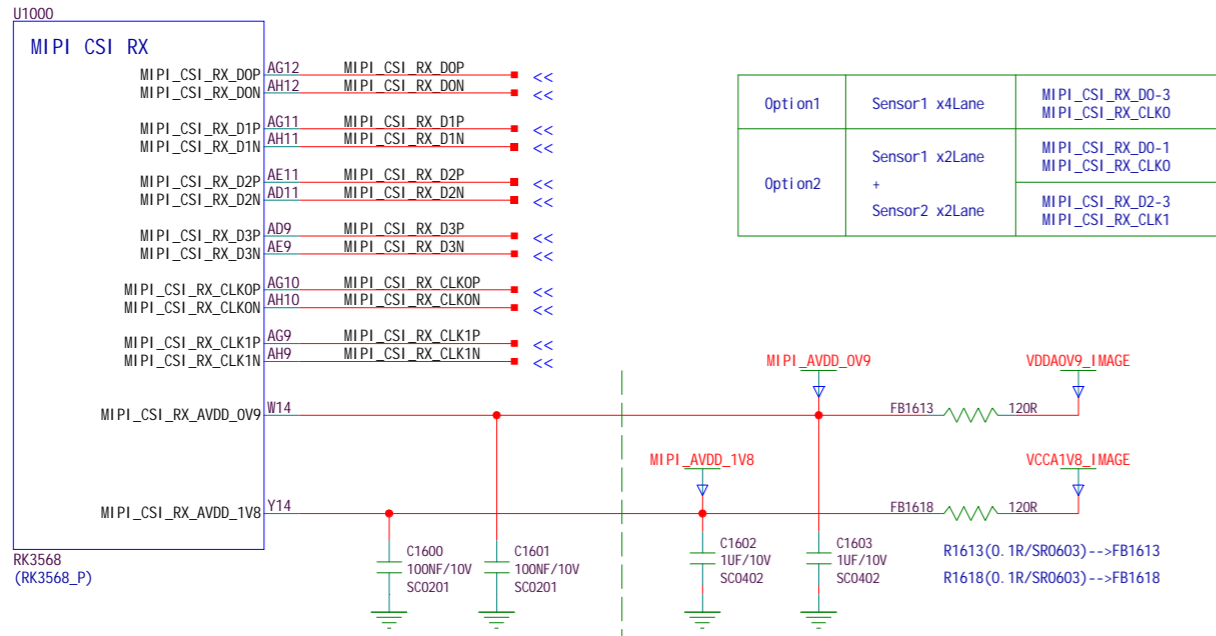


项目:	RK3568 AI Controller	页码:	15 OF 40
模块:	RK3568_SARADC/GPIO	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

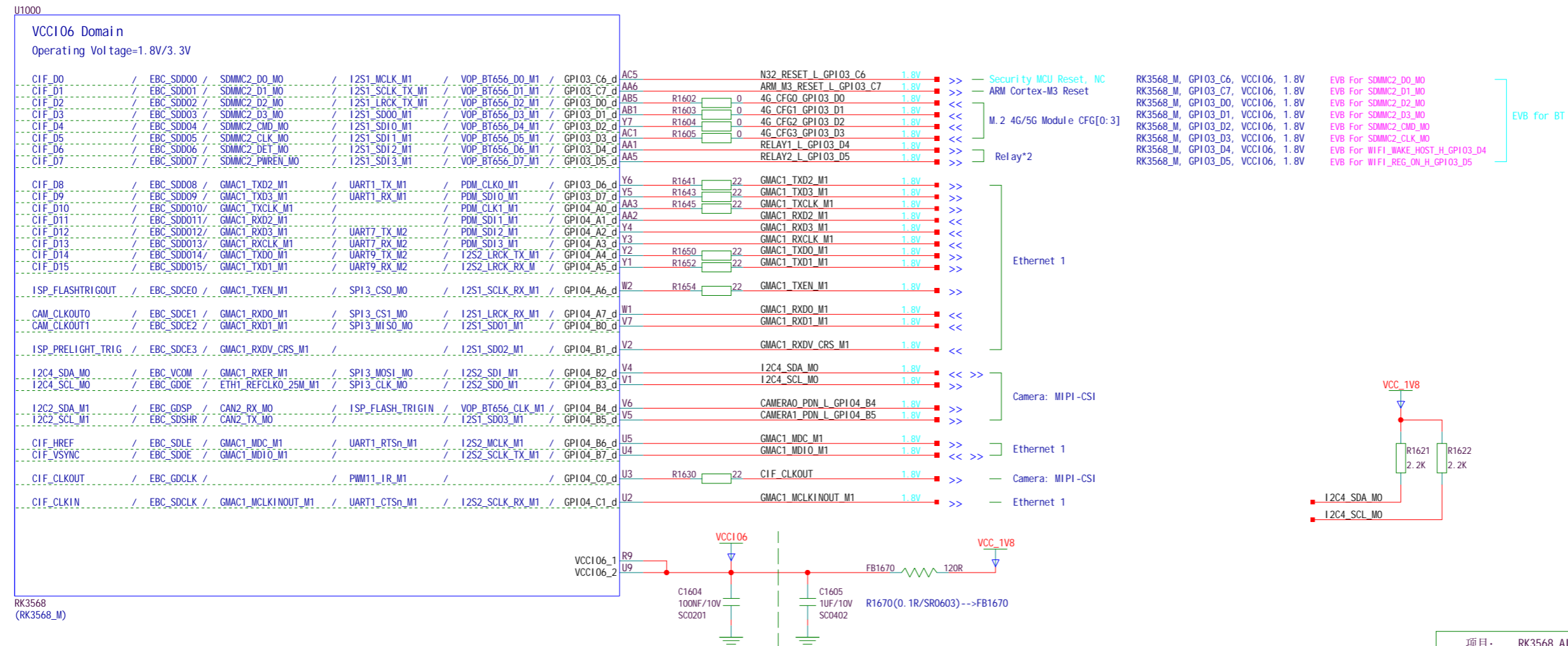
RK3568_P (MIPI_CSI_RX)

RK3568_VI Interface

16



RK3568_M GMAC1 (VCCI06 Domain)



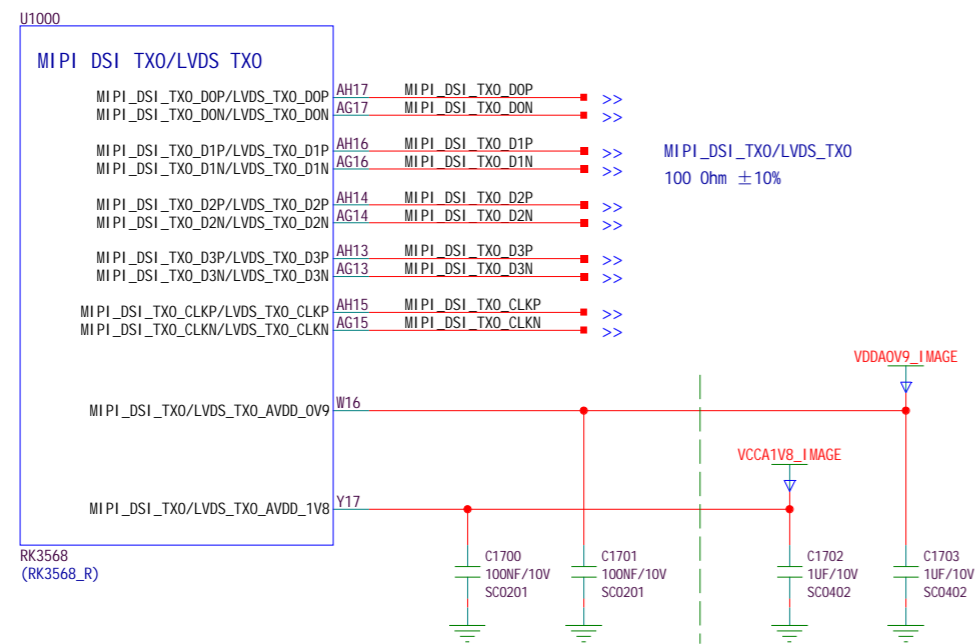
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.

Other caps should be placed close to the U1000 package

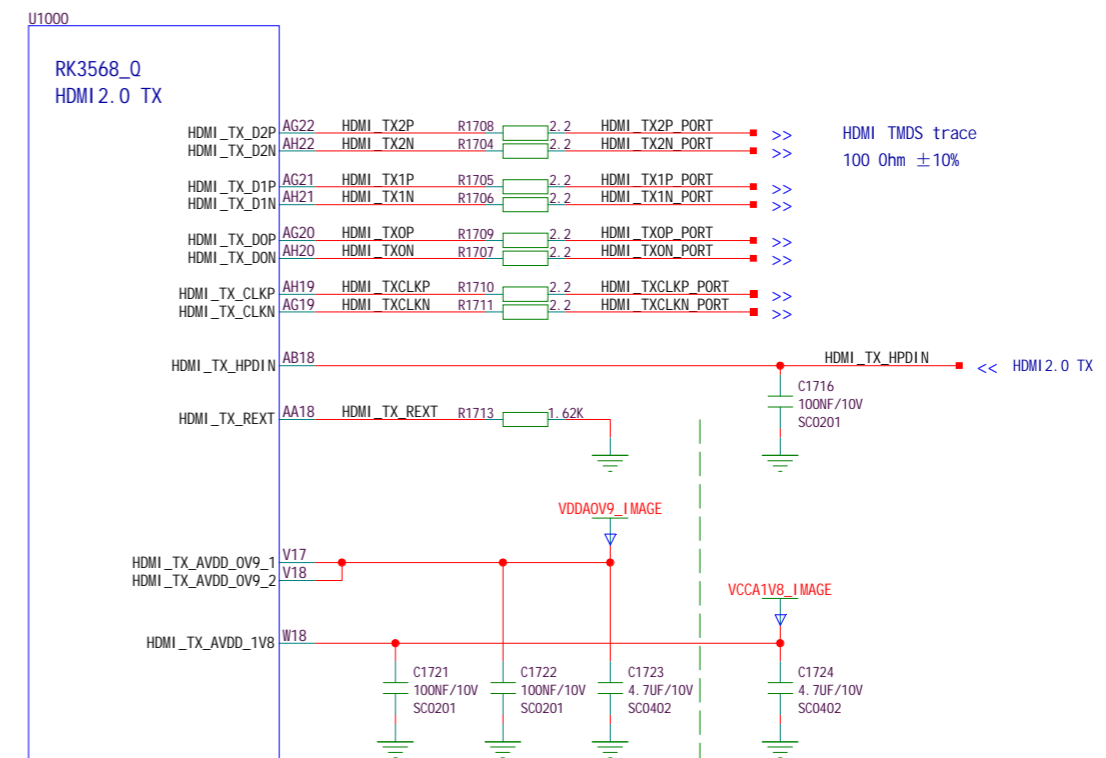
项目:	RK3568 AI Controller	页码:	16 OF 40
模块:	RK3568_VI INTERFACE	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

RK3568_R (MIPI_DSI_TX0 / LVDS_TX0)

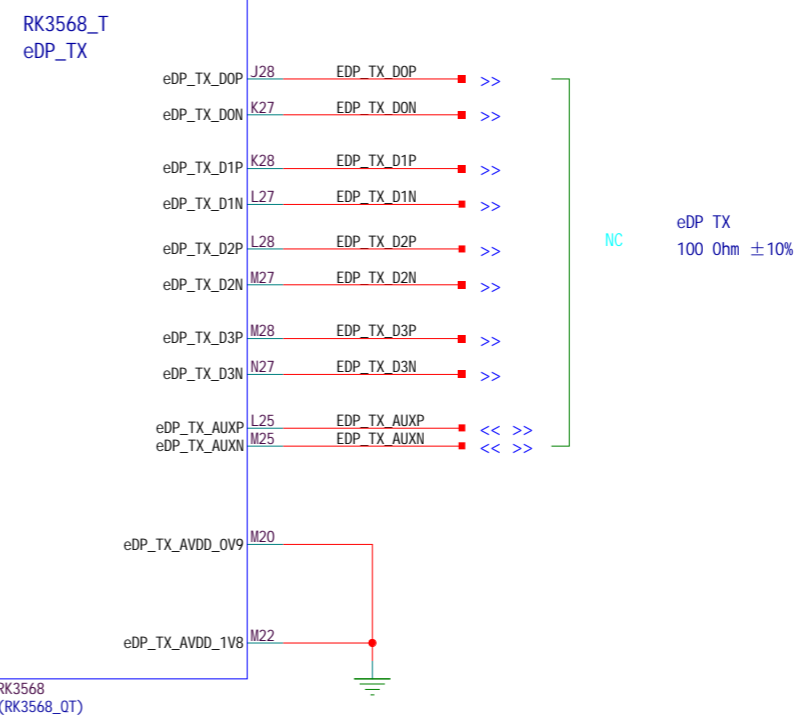
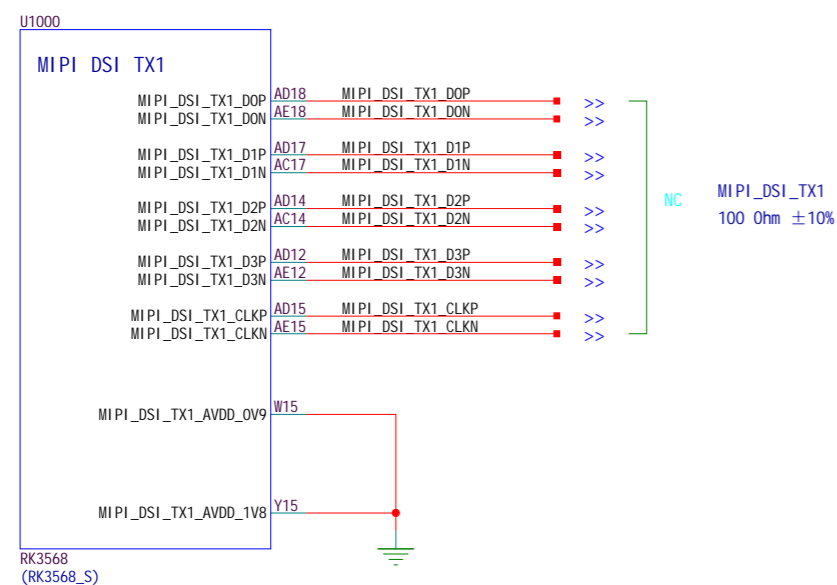


RK3568_Q (HDMI 2.0 TX) and RK3568_T (eDP TX)

17



RK3568_S (MIPI_DSI_TX1)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

项目:	RK3568 AI Controller	页码:	17 OF 40
模块:	RK3568_V0 INTERFACE_1	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

RK3568_L RK3568 V0 Interface 2 (VCCI05 Domain)

18

U1000

VCCI05 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/	VOP_BT656_D0_M0	/	SPI0_MISO_M1	/	PCIE20_CLKREQn_M1	/	I2S1_MCLK_M2	/	GPIO2_D0_d
LCDC_D1	/	VOP_BT656_D1_M0	/	SPI0_MOSI_M1	/	PCIE20_WAKEn_M1	/	I2S1_SCLK_TX_M2	/	GPIO2_D1_d
LCDC_D2	/	VOP_BT656_D2_M0	/	SPI0_CS0_M1	/	PCIE30X1_CLKREQn_M1	/	I2S1_LRCK_TX_M2	/	GPIO2_D2_d
LCDC_D3	/	VOP_BT656_D3_M0	/	SPI0_CLK_M1	/	PCIE30X1_WAKEn_M1	/	I2S1_SDIO_M2	/	GPIO2_D3_d
LCDC_D4	/	VOP_BT656_D4_M0	/	SPI2_CS1_M1	/	PCIE30X2_CLKREQn_M1	/	I2S1_SD11_M2	/	GPIO2_D4_d
LCDC_D5	/	VOP_BT656_D5_M0	/	SPI2_CS0_M1	/	PCIE30X2_WAKEn_M1	/	I2S1_SD12_M2	/	GPIO2_D5_d
LCDC_D6	/	VOP_BT656_D6_M0	/	SPI2_MOSI_M1	/	PCIE30X2_PERSTn_M1	/	I2S1_SD13_M2	/	GPIO2_D6_d
LCDC_D7	/	VOP_BT656_D7_M0	/	SPI2_MISO_M1	/	UART8_TX_M1	/	I2S1_SD00_M2	/	GPIO2_D7_d
LCDC_CLK	/	VOP_BT656_CLK_M0	/	SPI2_CLK_M1	/	UART8_RX_M1	/	I2S1_SD01_M2	/	GPIO3_A0_d
LCDC_D8	/	VOP_BT1120_D0	/	SPI1_CS0_M1	/	PCIE30X1_PERSTn_M1	/	SDMMC2_D0_M1	/	GPIO3_A1_d
LCDC_D9	/	VOP_BT1120_D1	/	GMAC1_TXD2_M0	/	I2S3_MCLK_M0	/	SDMMC2_D1_M1	/	GPIO3_A2_d
LCDC_D10	/	VOP_BT1120_D2	/	GMAC1_TXD3_M0	/	I2S3_SCLK_M0	/	SDMMC2_D2_M1	/	GPIO3_A3_d
LCDC_D11	/	VOP_BT1120_D3	/	GMAC1_RXD2_M0	/	I2S3_LRCK_M0	/	SDMMC2_D3_M1	/	GPIO3_A4_d
LCDC_D12	/	VOP_BT1120_D4	/	GMAC1_RXD3_M0	/	I2S3_SDO_M0	/	SDMMC2_CMD_M1	/	GPIO3_A5_d
LCDC_D13	/	VOP_BT1120_CLK	/	GMAC1_TXCLK_M0	/	I2S3_SDI_M0	/	SDMMC2_CLK_M1	/	GPIO3_A6_d
LCDC_D14	/	VOP_BT1120_D5	/	GMAC1_RXCLK_M0	/		/	SDMMC2_DET_M1	/	GPIO3_A7_d
LCDC_D15	/	VOP_BT1120_D6	/	ETH1_REFCLK0_25M_M0	/		/	SDMMC2_PWRn_M1	/	GPIO3_B0_d
LCDC_D16	/	VOP_BT1120_D7	/	GMAC1_RXD0_M0	/	UART4_RX_M1	/	PWM8_M0	/	GPIO3_B1_d
LCDC_D17	/	VOP_BT1120_D8	/	GMAC1_RXD1_M0	/	UART4_TX_M1	/	PWM9_M0	/	GPIO3_B2_d
LCDC_D18	/	VOP_BT1120_D9	/	GMAC1_RXDV_CRS_M0	/	I2C5_SCL_M0	/	PDM_SD10_M2	/	GPIO3_B3_d
LCDC_D19	/	VOP_BT1120_D10	/	GMAC1_RXER_M0	/	I2C5_SDA_M0	/	PDM_SD11_M2	/	GPIO3_B4_d
LCDC_D20	/	VOP_BT1120_D11	/	GMAC1_TXD0_M0	/	I2C3_SCL_M1	/	PWM10_M0	/	GPIO3_B5_d
LCDC_D21	/	VOP_BT1120_D12	/	GMAC1_TXD1_M0	/	I2C3_SDA_M1	/	PWM11_IR_M0	/	GPIO3_B6_d
LCDC_D22	/	PWM12_M0	/	GMAC1_TXEN_M0	/	UART3_TX_M1	/	PDM_SD12_M2	/	GPIO3_B7_d
LCDC_D23	/	PWM13_M0	/	GMAC1_MCLK1NOUT_M0	/	UART3_RX_M1	/	PDM_SD13_M2	/	GPIO3_C0_d
LCDC_HSYNC	/	VOP_BT1120_D13	/	SPI1_MOSI_M1	/	PCIE20_PERSTn_M1	/	I2S1_SD02_M2	/	GPIO3_C1_d
LCDC_VSYNC	/	VOP_BT1120_D14	/	SPI1_MISO_M1	/	UART5_TX_M1	/	I2S1_SD03_M2	/	GPIO3_C2_d
LCDC_DEN	/	VOP_BT1120_D15	/	SPI1_CLK_M1	/	UART5_RX_M1	/	I2S1_SCLK_RX_M2	/	GPIO3_C3_d
PWM14_M0	/	VOP_PWM_M1	/	GMAC1_MDC_M0	/	UART7_TX_M1	/	PDM_CLK1_M2	/	GPIO3_C4_d
PWM15_IR_M0	/	SPDIF_TX_M1	/	GMAC1_MDIO_M0	/	UART7_RX_M1	/	I2S1_LRCK_RX_M2	/	GPIO3_C5_d

RK3568
(RK3568_L)

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.

Other caps should be placed close to the U1000 package

AG6	GMAC1_INT/PMEB_GPIO2_D0	3.3V	<<
AD7	GMAC1_RSTN_GPIO2_D1	3.3V	>>
AC8	GMAC0_INT/PMEB_GPIO2_D2	3.3V	<<
AC7	GMAC0_RSTN_GPIO2_D3	3.3V	>>
AF5	PCIE30X2_CLKREQn_M1	3.3V	<<
AF6	PCIE30X2_WAKEn_M1	3.3V	>>
AD6	PCIE30X2_PERSTn_M1	3.3V	<<
AH5	PCIE30X2_PRSTN_L_GPIO2_D7	3.3V	>>
AH4	4G_POWER_EN_L_GPIO3_A0	3.3V	>>
AB8	4G_POWER_KEY_L_GPIO3_A1	3.3V	>>
AE5	4G_RESET_L_GPIO3_A2	3.3V	>>
AG4	RK_DIN_0_GPIO3_A3	3.3V	<<
AF4	RK_DIN_1_GPIO3_A4	3.3V	<<
AH3	RK_DIN_2_GPIO3_A5	3.3V	<<
AG3	RK_DIN_3_GPIO3_A6	3.3V	<<
AH2	PCIECLKIC_OE_H_GPIO3_A7	3.3V	>>
AG2	ETH1_REFCLK0_25M_M0	3.3V	>>
AG1	UART4_RX_M1	3.3V	<<
AF2	UART4_TX_M1	3.3V	>>
AF1	I2C5_SCL_M0	3.3V	>>
AE1	I2C5_SDA_M0	3.3V	>>
AE2	R1806 0 MIPICAM1_RST_L_GPIO3_B5	3.3V	>>
AE3	R1807 0 MIPICAM0_RST_L_GPIO3_B6	3.3V	>>
AD4	R1805 22 UART3_TX_M1	3.3V	>>
AD2	UART3_RX_M1	3.3V	<<
AD1	RK_DIN_CTRL_GPIO3_C1	3.3V	<<
AA7	AUDIO_PA_FAULT_L_GPIO3_C2	3.3V	<<
AC4	AUDIO_PA_SD_H_GPIO3_C3	3.3V	>>
AC3	PWM14_M0	3.3V	>>
AC2	BUZZER_PWM15_IR_M0	3.3V	>>

Ethernet 1
Ethernet 0

mini PCIe (PCIe3.0 x 1Lanes)
RK3568_L, GPIO2_D7, Reset RK1808 , Active High

M.2 4G/5G Module Control
RK3568_L, GPIO3_A0, VCCI05, 3.3V EVB For BT_REG_ON_H_GPIO3_A0
RK3568_L, GPIO3_A1, VCCI05, 3.3V EVB For BT_WAKE_HOST_H_GPIO3_A1
RK3568_L, GPIO3_A2, VCCI05, 3.3V EVB For HOST_WAKE_BT_H_GPIO3_A2

RK Din *4 Channels
RK3568_L, GPIO3_A3, VCCI05, 3.3V EVB For I2S3_SCLK_M0
RK3568_L, GPIO3_A4, VCCI05, 3.3V EVB For I2S3_LRCK_M0
RK3568_L, GPIO3_A5, VCCI05, 3.3V EVB For I2S3_SDO_M0
RK3568_L, GPIO3_A6, VCCI05, 3.3V EVB For I2S3_SDI_M0

mini PCIe (PCIe3.0 x 1Lanes)
Ethernet 0

RS-232-2

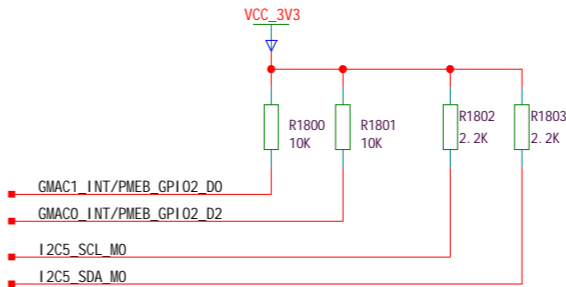
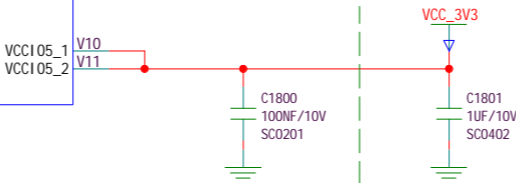
RTC

Camera: MIPI-CSI
RK3568_L, GPIO3_B5, VCCI05, 3.3V
RK3568_L, GPIO3_B6, VCCI05, 3.3V

RS-232-1

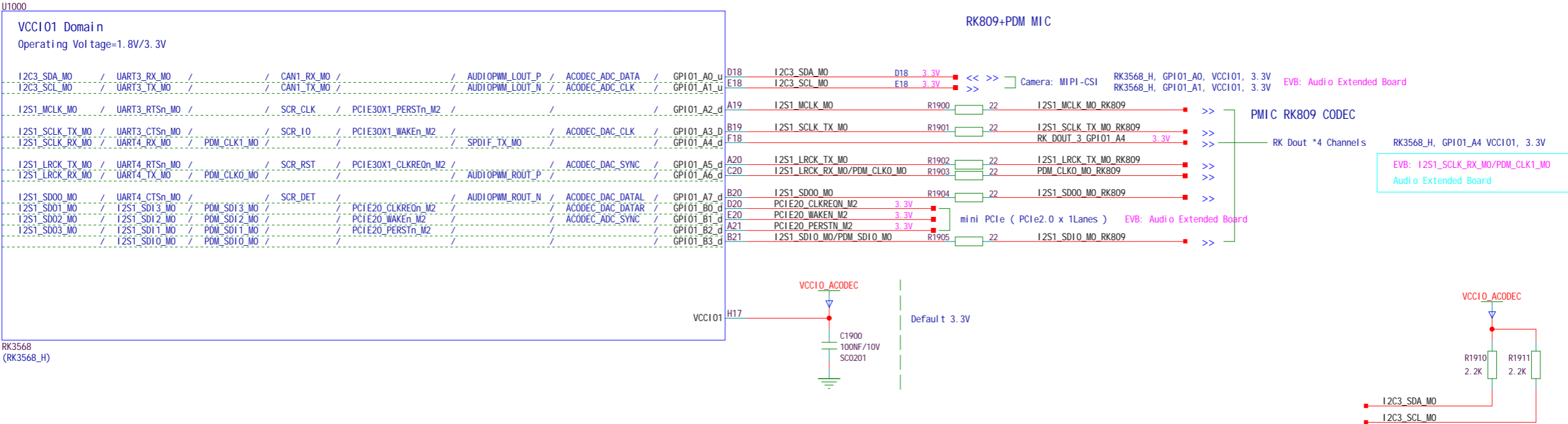
RK Din *4 Channels
RK3568_L, GPIO3_C1, VCCI05, 3.3V EVB For SENSOR_INT_L_GPIO3_C1
RK3568_L, GPIO3_C2, VCCI05, 3.3V EVB For HP_DET_L_GPIO3_C2
Audio Power Amplifier
RK3568_L, GPIO3_C3, VCCI05, 3.3V EVB For PA_EN_H_GPIO3_C3

Camera: MIPI-CSI
RK3568_L, GPIO3_C4, VCCI05, 3.3V
Buzzer
RK3568_L, GPIO3_C5, VCCI05, 3.3V EVB For Audio-S/PDIF TX Port



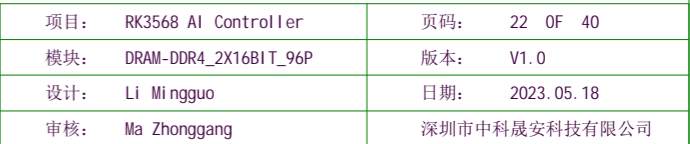
项目:	RK3568 AI Controller	页码:	18 OF 40
模块:	RK3568_V0 INTERFACE_2	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

RK3568_H RK3568 Audio Interface (VCCI01 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

项目：	RK3568 AI Controller	页码：	19 OF 40
模块：	RK3568_AUDIO INTERFACE	版本：	V1.0
设计：	Li Mingguo	日期：	2023.05.18
审核：	Ma Zhonggang		深圳市中科晟安科技有限公司



eMMC Flash

40

A

A

B

B

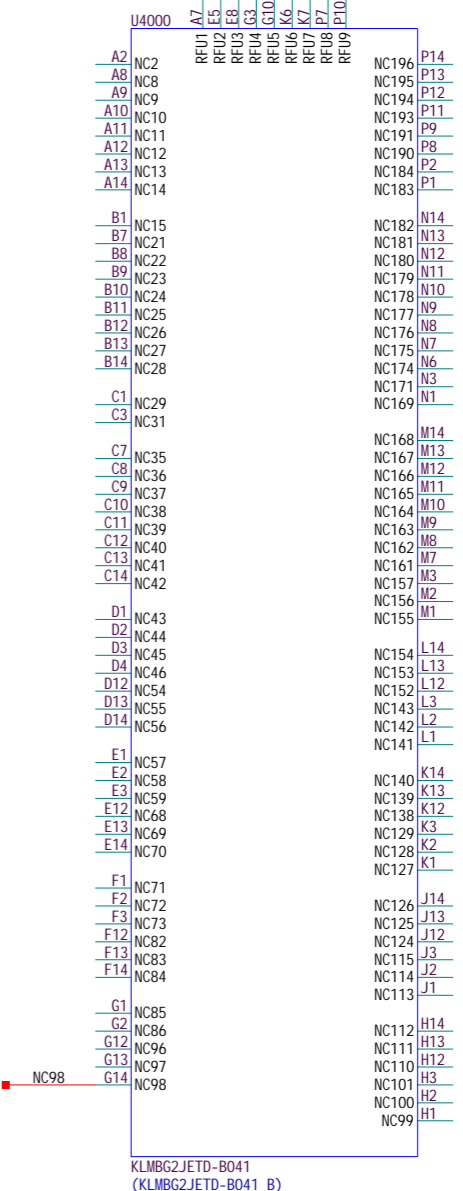
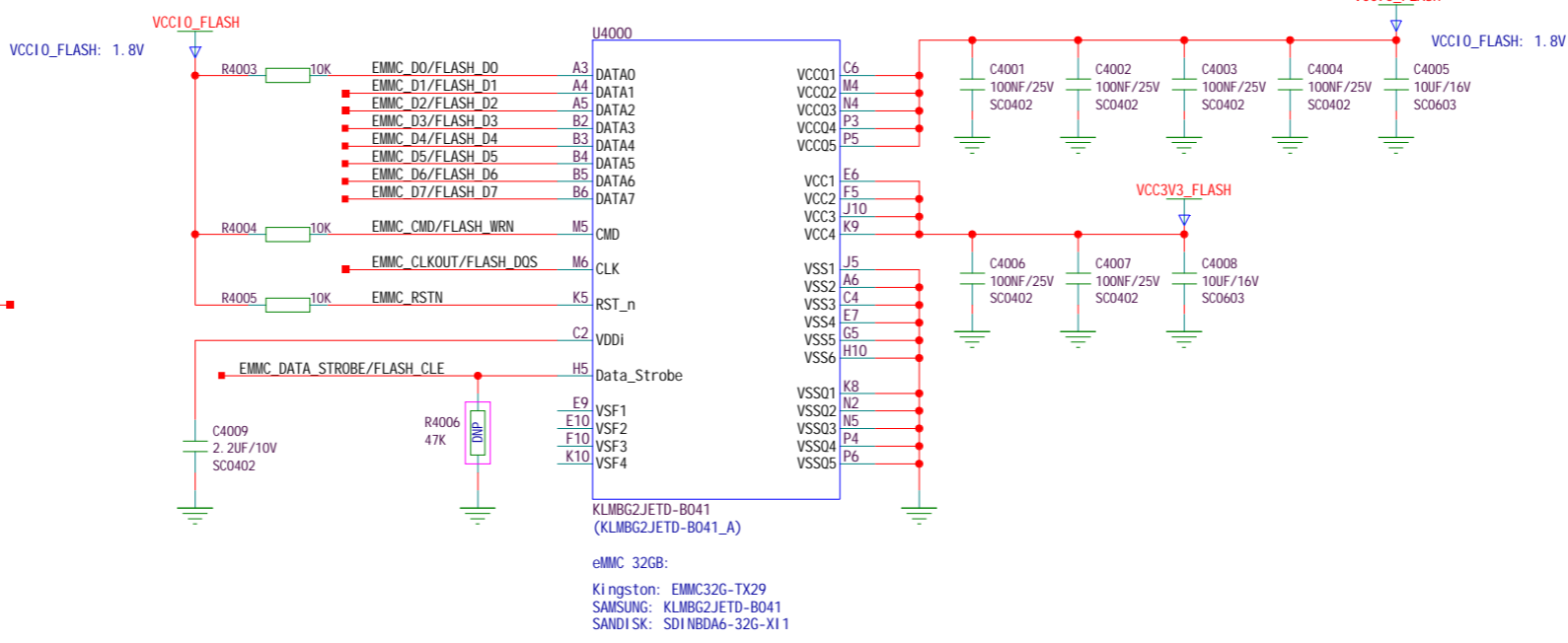
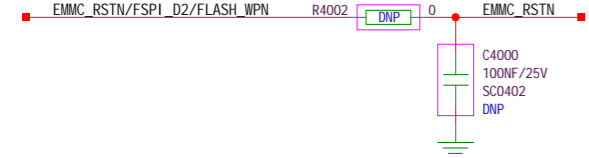
C

C

D

D

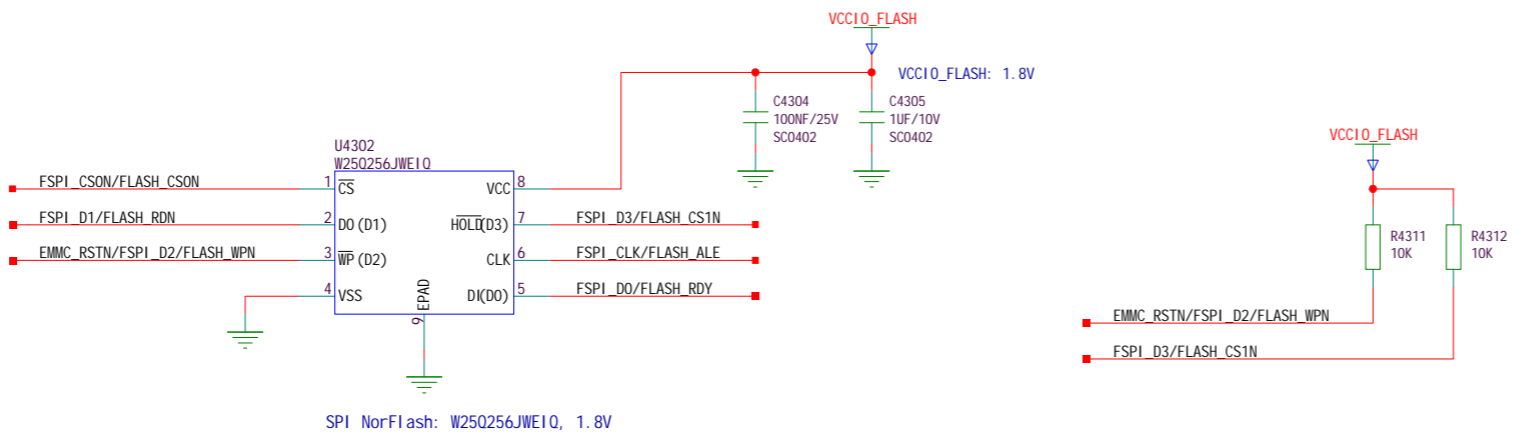
- << >> EMMC_D0/FLASH_D0
- << >> EMMC_D1/FLASH_D1
- << >> EMMC_D2/FLASH_D2
- << >> EMMC_D3/FLASH_D3
- << >> EMMC_D4/FLASH_D4
- << >> EMMC_D5/FLASH_D5
- << >> EMMC_D6/FLASH_D6
- << >> EMMC_D7/FLASH_D7
- << >> EMMC_CMD/FLASH_WRN
- >> EMMC_CLKOUT/FLASH_DQS
- << >> EMMC_DATA_STROBE/FLASH_CLE
- >> EMMC_RSTN/FSPI_D2/FLASH_WPN



SPI Flash

43

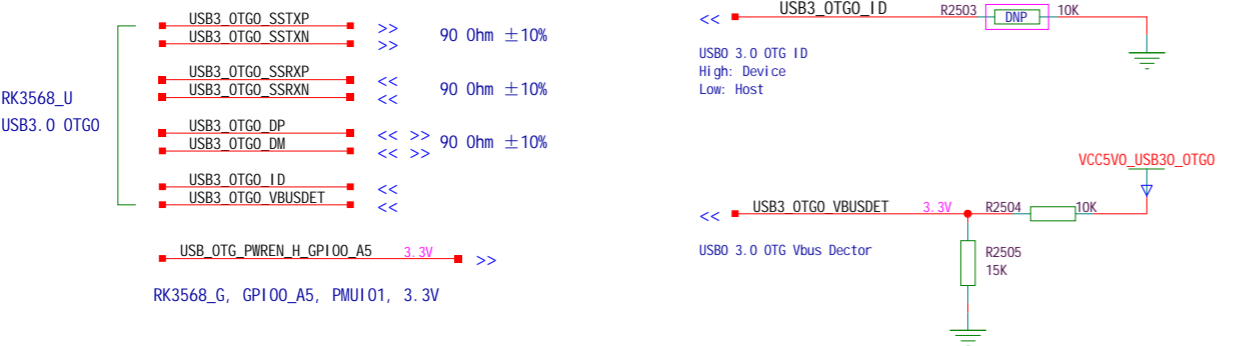
- >> FSPI_CLK/FLASH_ALE
- >> FSPI_D0/FLASH_RDY
- >> FSPI_D1/FLASH_RDN
- >> EMMC_RSTN/FSPI_D2/FLASH_WPN
- >> FSPI_D3/FLASH_CS1N
- >> FSPI_CSON/FLASH_CSON



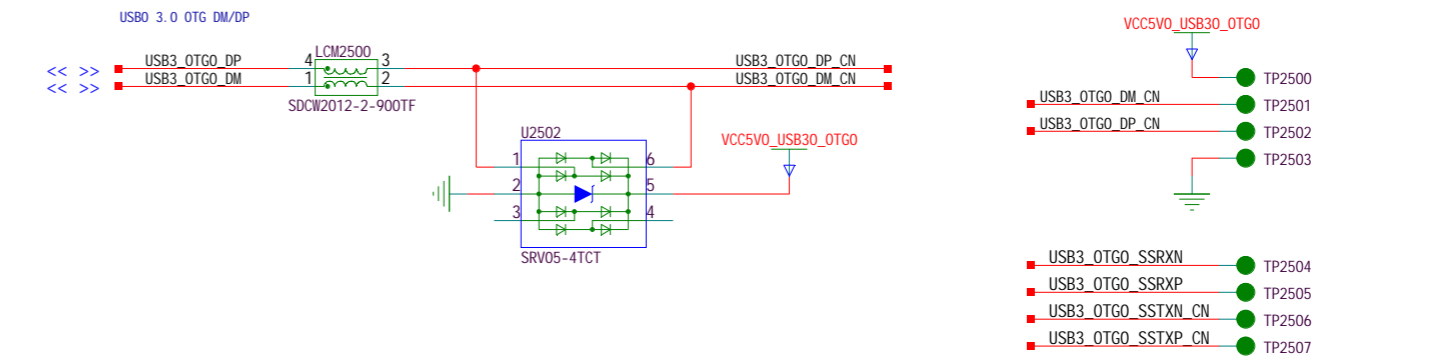
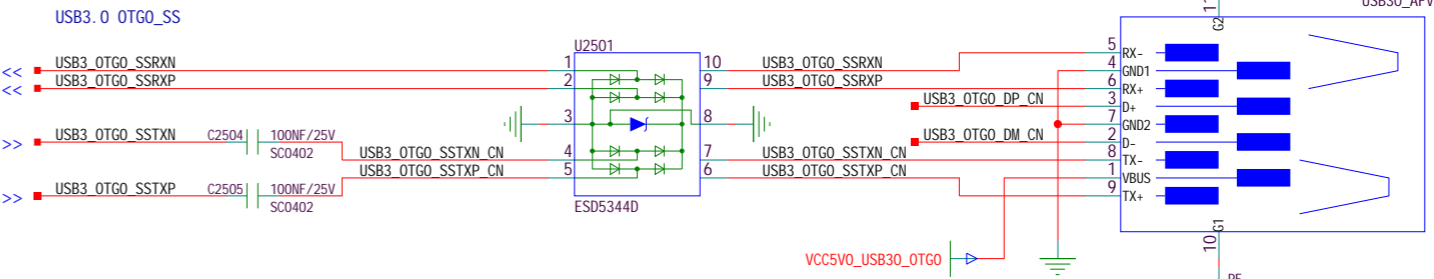
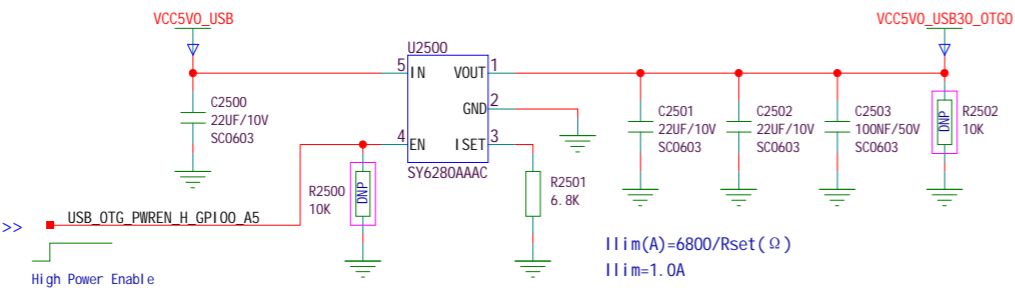
项目:	RK3568 AI Controller	页码:	23 OF 40
模块:	EMMC FLASH / SPI FLASH	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

USB 3.0 OTG

A

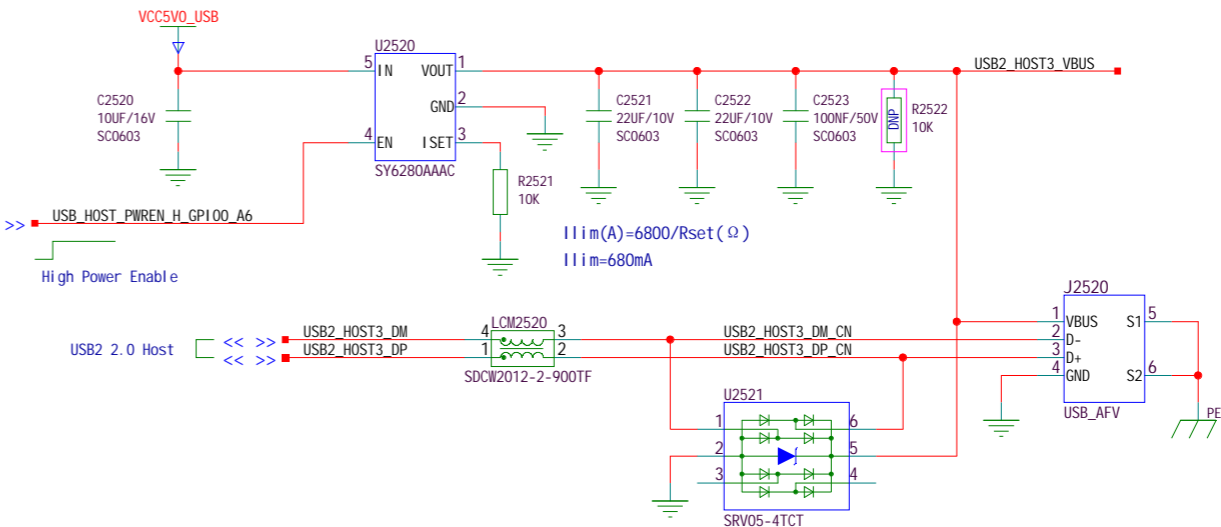
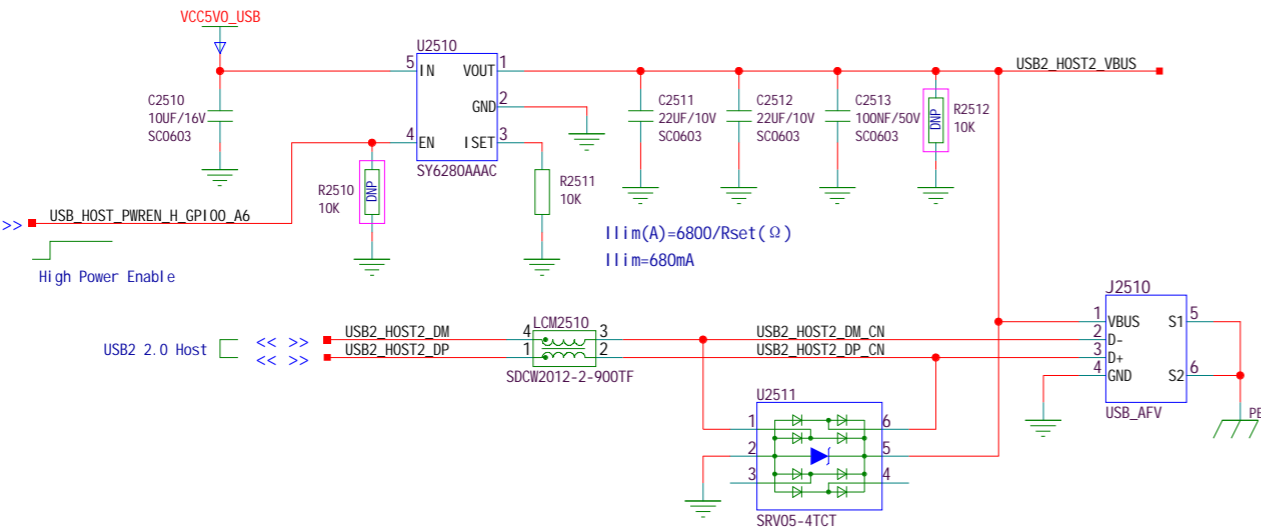


B



USB 2.0 Host*2

C



D



项目:	RK3568 AI Controller	页码:	25 OF 40
模块:	USB2/USB3 PORT	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

A

B

C

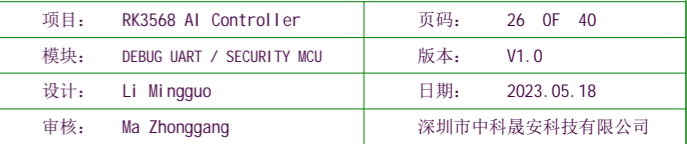
D

B



D

3



Camera: MIPI-CSI

28

A

A

B

B

C

C

D

D

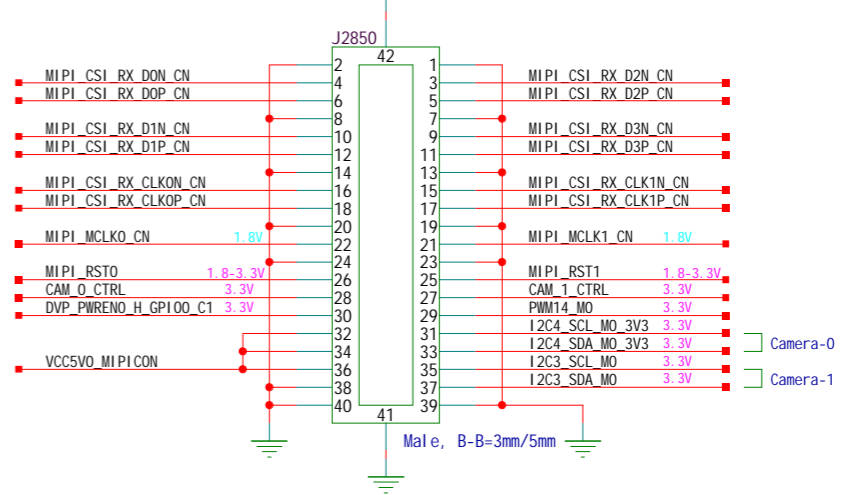
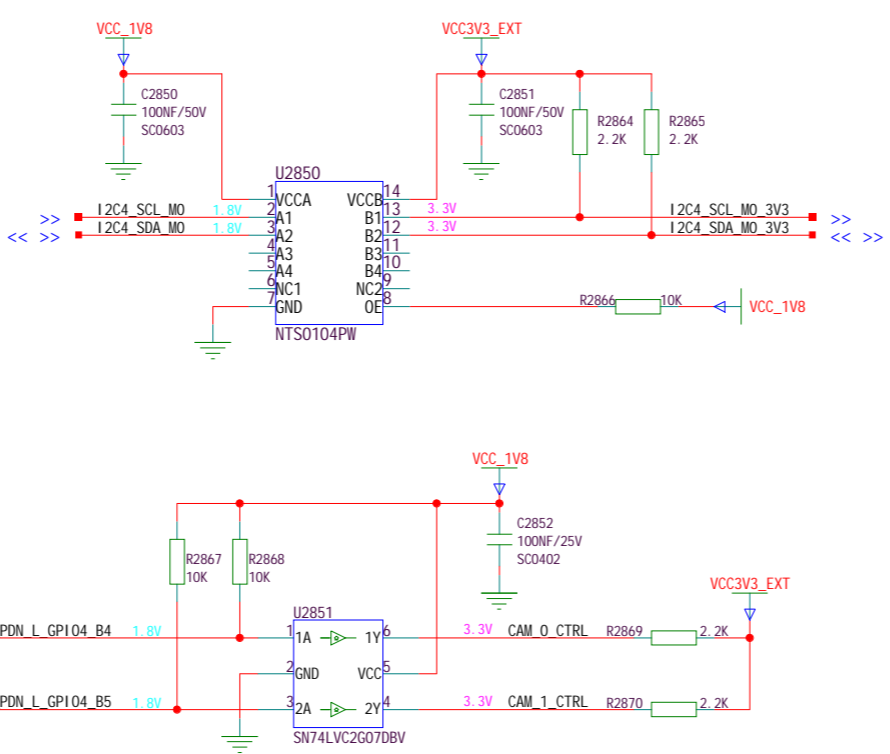
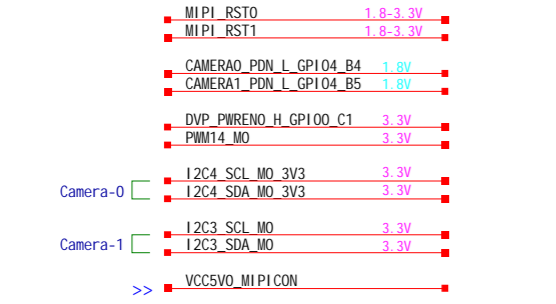
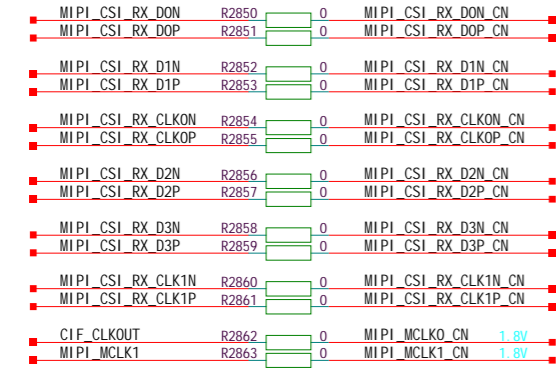
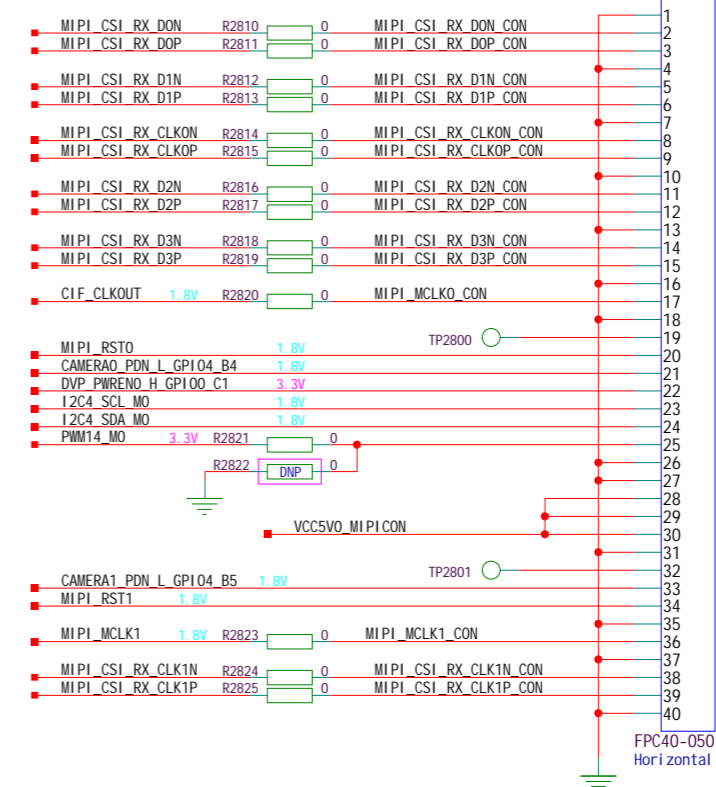
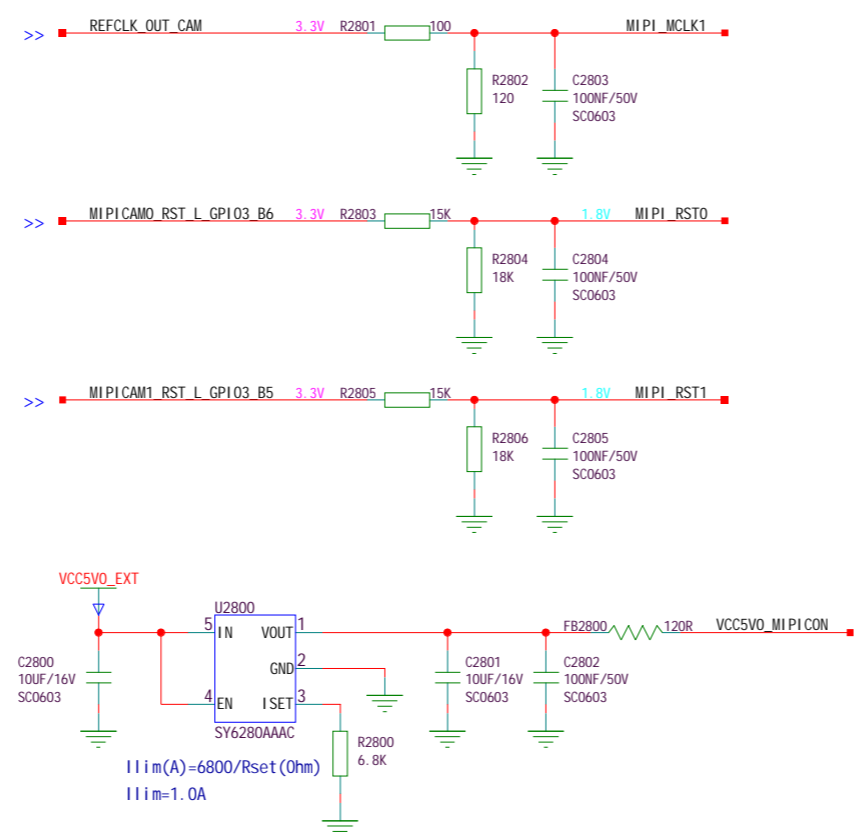
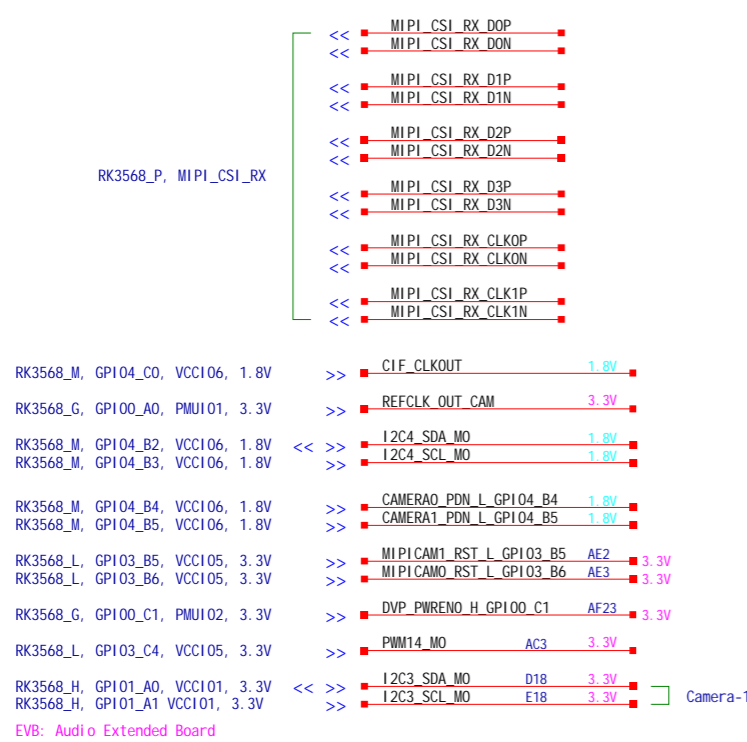
Camera (MIPI-CSI x2Lane) x2 Extend

285+

MIPI-CSI FPC Pin List

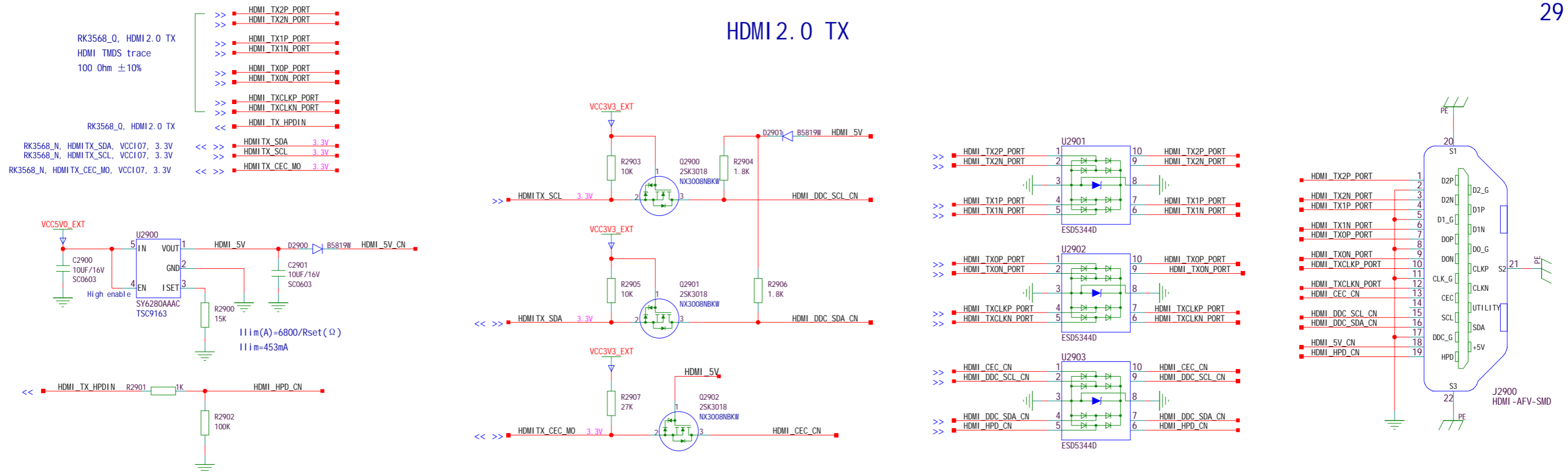
Pin 1:	GND
Pin 2:	DON
Pin 3:	DOP
Pin 4:	GND
Pin 5:	D1N
Pin 6:	D1P
Pin 7:	GND
Pin 8:	CLKON
Pin 9:	CLKOP
Pin 10:	GND
Pin 11:	D2N
Pin 12:	D2P
Pin 13:	GND
Pin 14:	D3N
Pin 15:	D3P
Pin 16:	GND
Pin 17:	MIPI_MCLK0 1.8V
Pin 18:	GND
Pin 19:	1V8_OUT
Pin 20:	MIPI_RST0 1.8V
Pin 21:	MIPI_PDN0 1.8V
Pin 22:	MIPI_PWREN0 1.8V~3.3V
Pin 23:	I2C_SCL 1.8V
Pin 24:	I2C_SDA 1.8V
Pin 25:	GND/FSYNC_IN 1.8V
Pin 26:	GND
Pin 27:	GND
Pin 28:	5V0_IN
Pin 29:	5V0_IN
Pin 30:	5V0_IN
Pin 31:	GND
Pin 32:	MIPI_PWREN1 1.8V~3.3V
Pin 33:	MIPI_PDN1 1.8V
Pin 34:	MIPI_RST1 1.8V
Pin 35:	GND
Pin 36:	MIPI_MCLK1 1.8V
Pin 37:	GND
Pin 38:	CLKIN
Pin 39:	CLKIN
Pin 40:	GND

FPC40-050-SMD
Horizontal SMT, 0.5mm Pitch, Bottom Contact Type

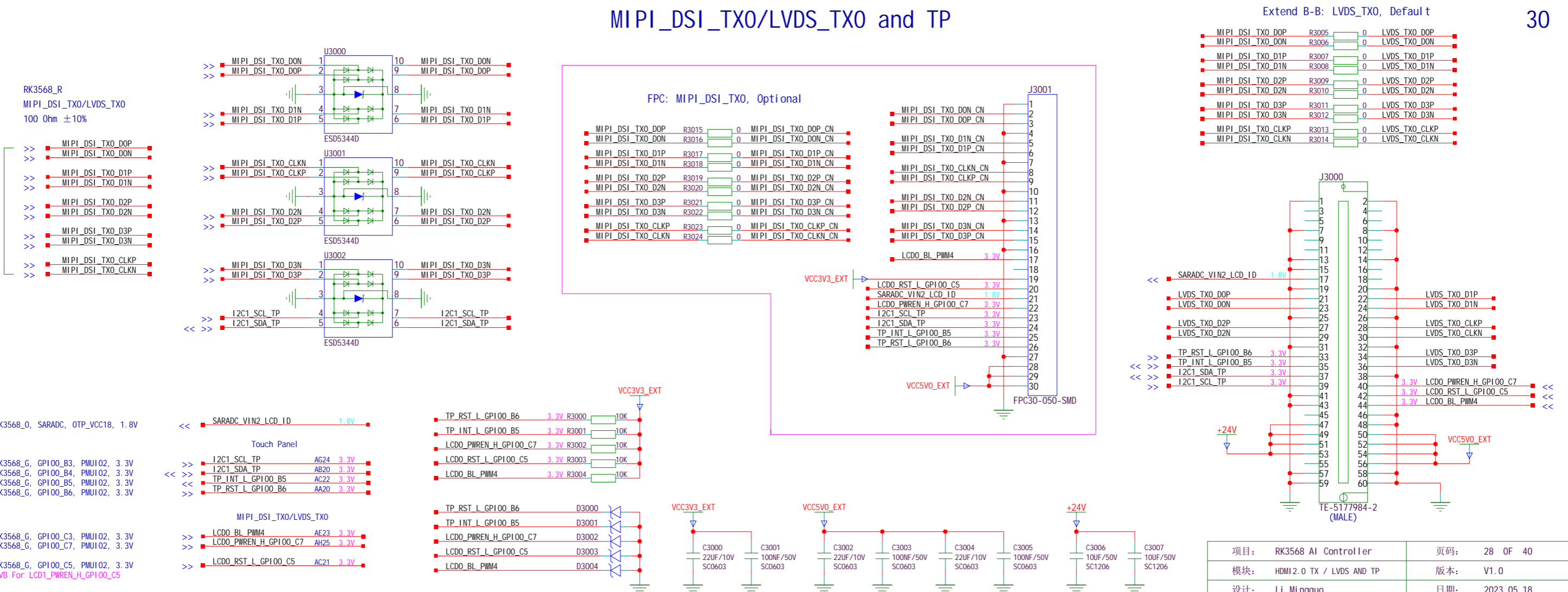


项目:	RK3568 AI Controller	页码:	27 OF 40
模块:	CAMERA MIPI-CSI	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

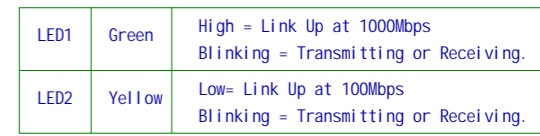
HDMI 2.0 TX



MIPI_DSI_TX0/LVDS_TX0 and TP



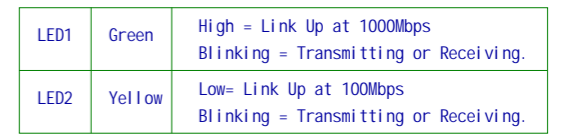
项目:	RK3568 AI Controller	页码:	28 OF 40
模块:	HDMI 2.0 TX / LVDS AND TP	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司



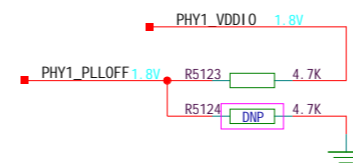
PHY Address Configuration, PHY Address = 001



项目:	RK3568 AI Controller	页码:	29 OF 40
模块:	RGMI I ETHERNET 0	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang	深圳市中科晟安科技有限公司	



Pul I - up to disable PLL @ ALDPS mode.



项目:	RK3568 AI Controller	页码:	30 OF 40
模块:	RGMI1 ETHERNET 1	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang	深圳市中科晟安科技有限公司	

Audi o Power Ampl i fi er

A

A

B

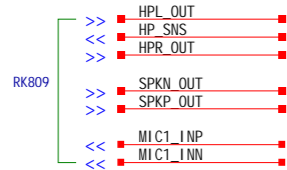
B

C

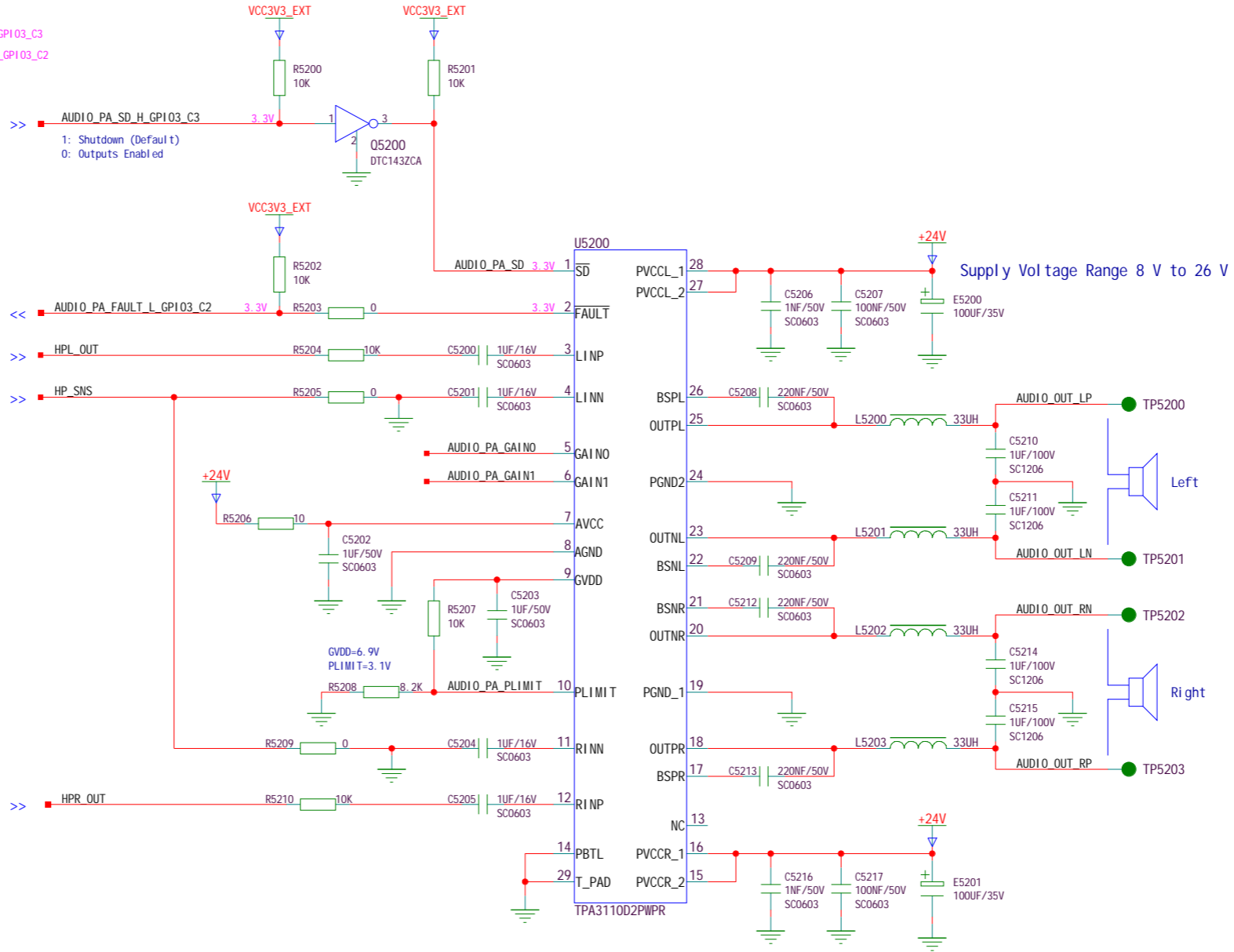
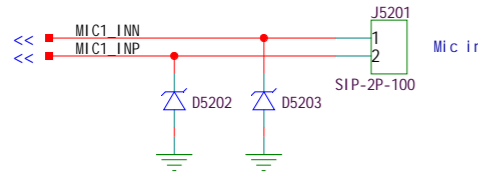
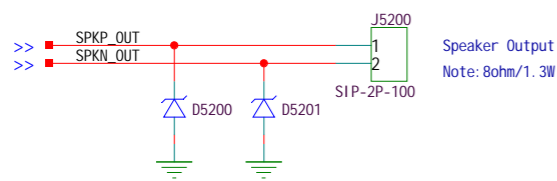
C

D

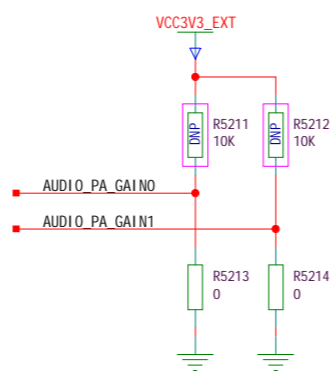
D



RK3568_L, GPIO3_C2, VCC105, 3.3V >> AUDIO_PA_SD_H_GPIO3_C3 AC4 3.3V EVB For PA_EN_H_GPIO3_C3
RK3568_L, GPIO3_C3, VCC105, 3.3V << AUDIO_PA_FAULT_L_GPIO3_C2 AA7 3.3V EVB For HP_DET_L_GPIO3_C2



PLIMIT Typical Operation			
Test Conditions	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (Vp-p)
PVCC=24V, Vin=1Vrms RL=8Ω, Gain=20dB	3.00	10	23



Gain Setting			
GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

项目:	RK3568 AI Controller	页码:	31 OF 40
模块:	AUDIO POWER AMPLIFIER	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

85 Ohm $\pm 10\%$



Optional

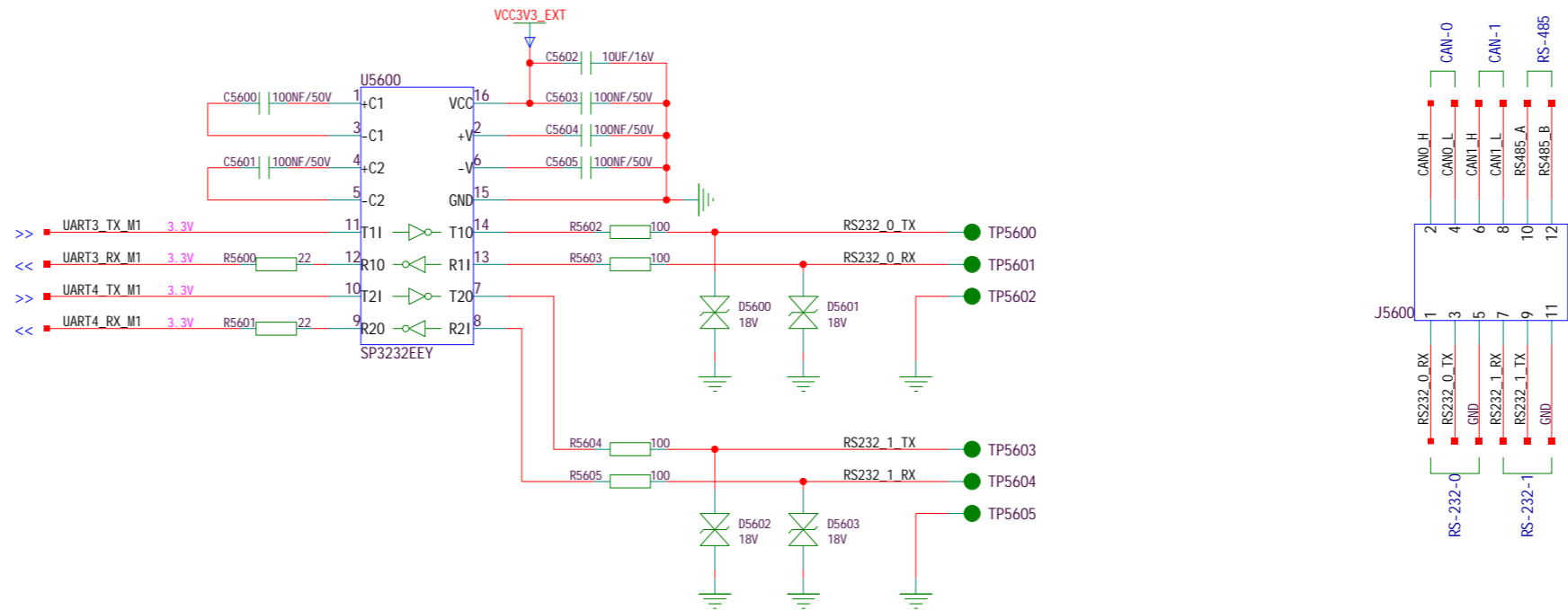


0

项目:	RK3568 AI Controller	页码:	33 OF 40
模块:	M.2 4G AND 5G MODULE	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang	深圳市中科晟安科技有限公司	

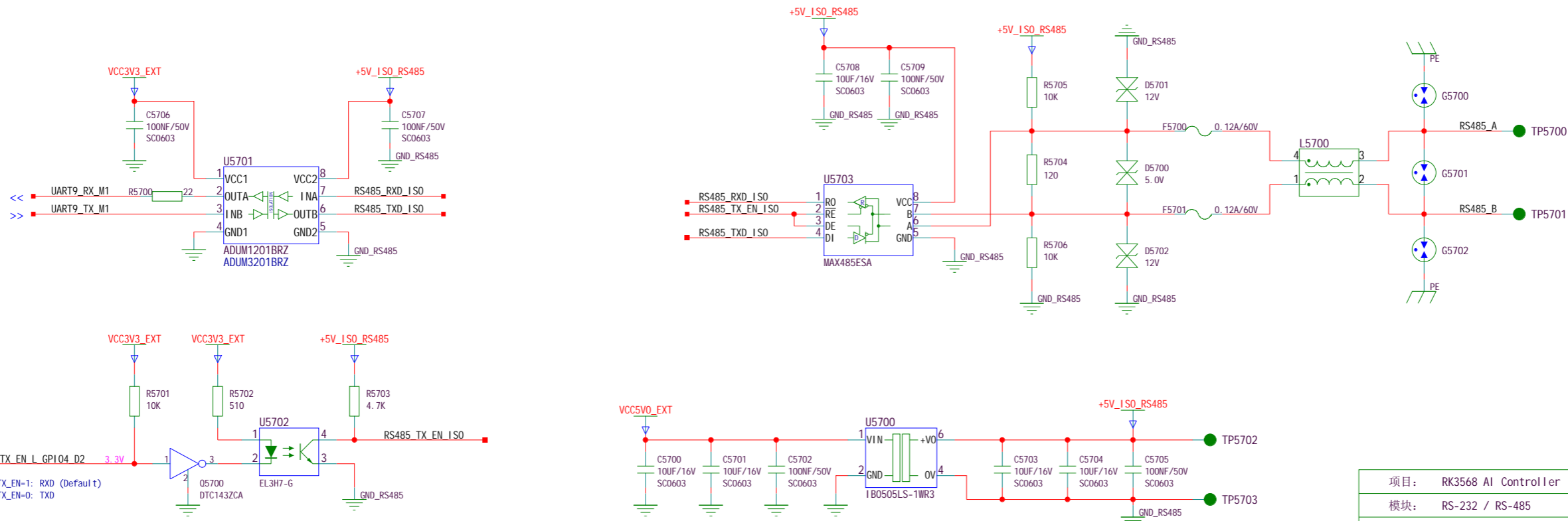
RS-232 *2

RK3568_L, GPIO3_B7, VCC105, 3.3V >> UART3_TX_M1 AD4 3.3V
RK3568_L, GPIO3_C0, VCC105, 3.3V << UART3_RX_M1 AD2 3.3V RS-232-1
RK3568_L, GPIO3_B2, VCC105, 3.3V >> UART4_TX_M1 AF2 3.3V
RK3568_L, GPIO3_B1, VCC105, 3.3V << UART4_RX_M1 AG1 3.3V RS-232-2



RS-485

RK3568_N, GPIO4_C5, VCC107, 3.3V >> UART9_TX_M1 AD8 3.3V
RK3568_N, GPIO4_C6, VCC107, 3.3V << UART9_RX_M1 AE8 3.3V RS-485
RK3568_N, GPIO4_D2, VCC107, 3.3V >> RS485_TX_EN_L_GPIO4_D2 AB9 3.3V RS-485_DIR EVB for CIF,EBC,RCMI1,BT656

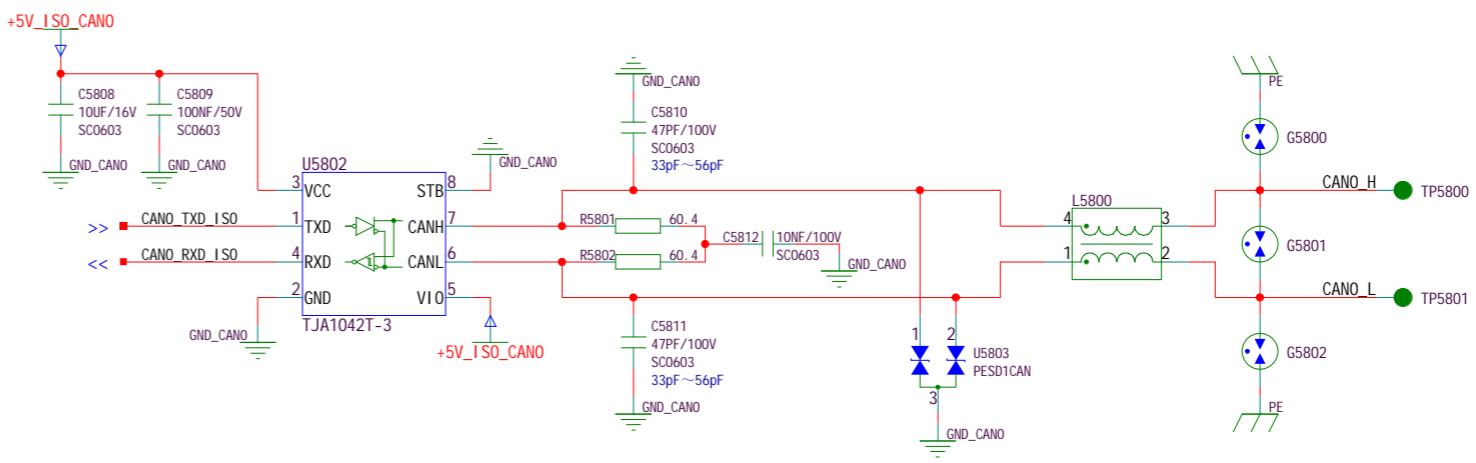
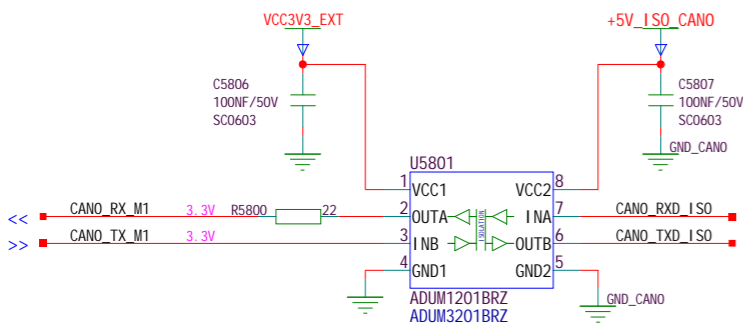
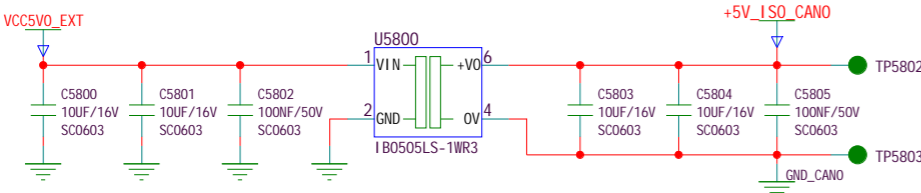


项目:	RK3568 AI Controller	页码:	34 OF 40
模块:	RS-232 / RS-485	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

CAN Bus - 0

58

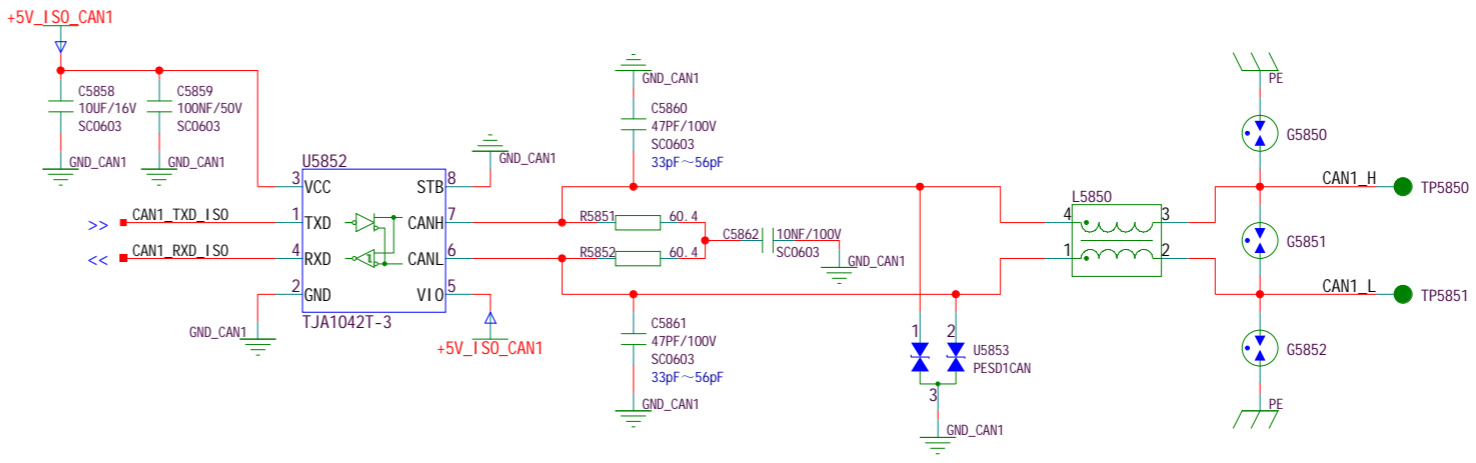
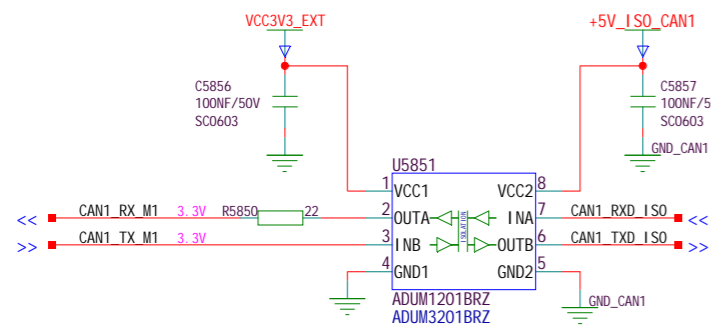
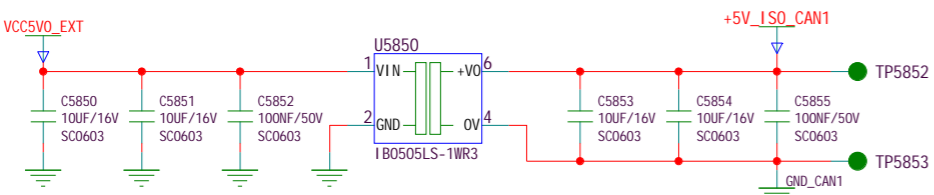
RK3568_J, GP102_A1, VCC103, 3.3V >> CANO_TX_M1 H27 3.3V
RK3568_J, GP102_A2, VCC103, 3.3V << CANO_RX_M1 H28 3.3V



CAN Bus - 1

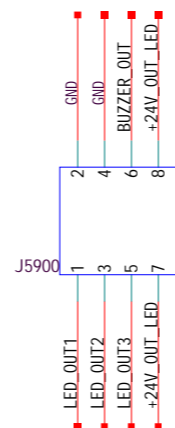
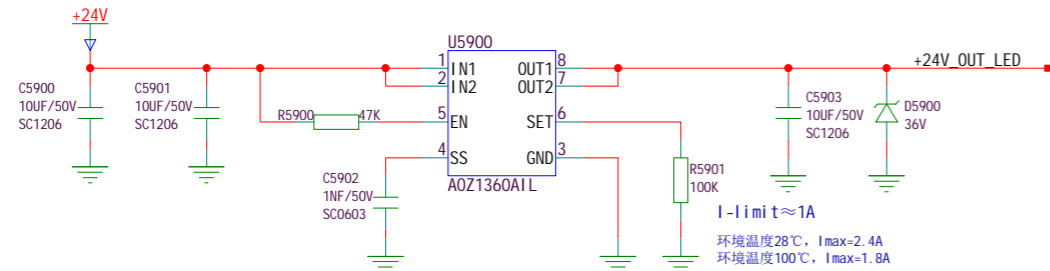
585+

RK3568_N, GP104_C3, VCC107, 3.3V >> CAN1_TX_M1 AA11 3.3V
RK3568_N, GP104_C2, VCC107, 3.3V << CAN1_RX_M1 AF8 3.3V

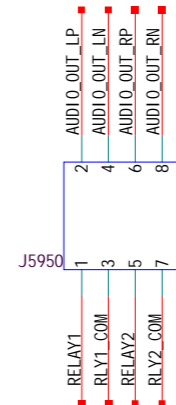


项目:	RK3568 AI Controller	页码:	35 OF 40
模块:	CAN BUS	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

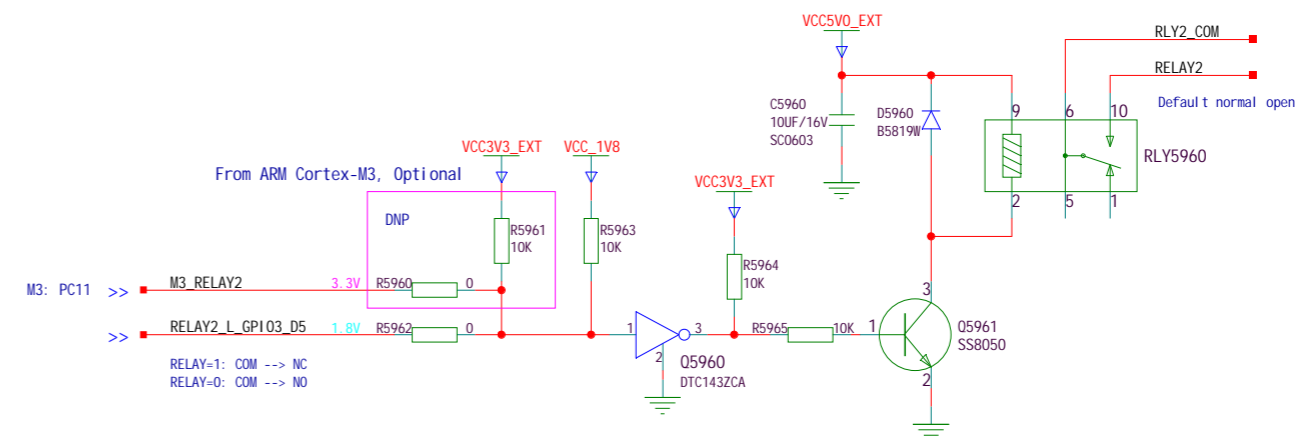
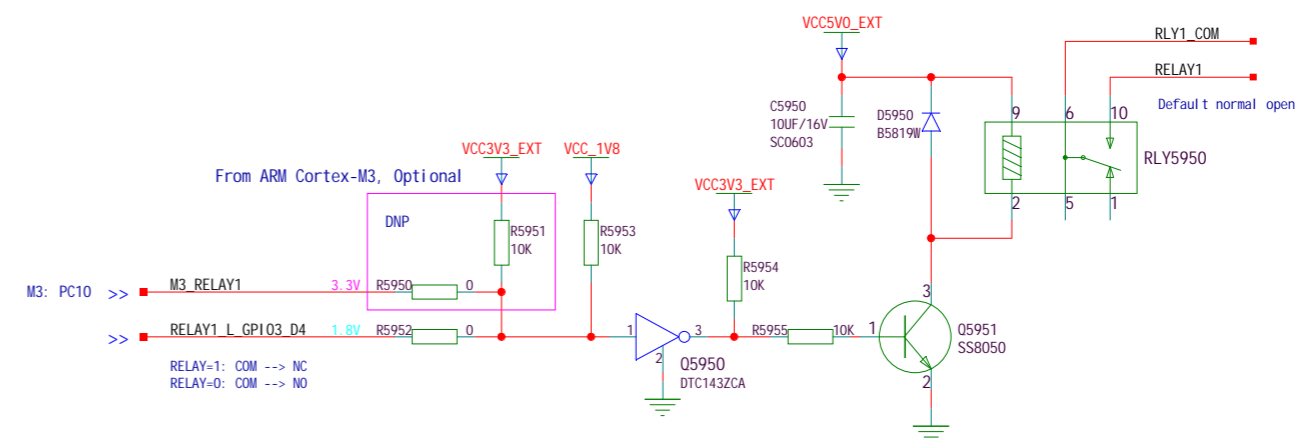
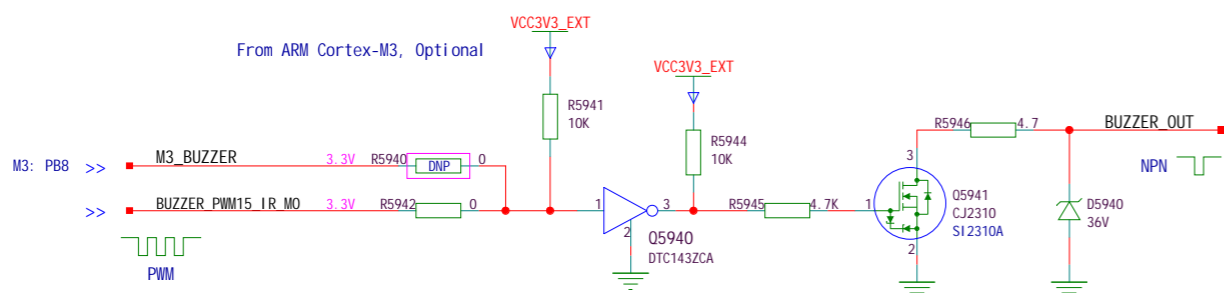
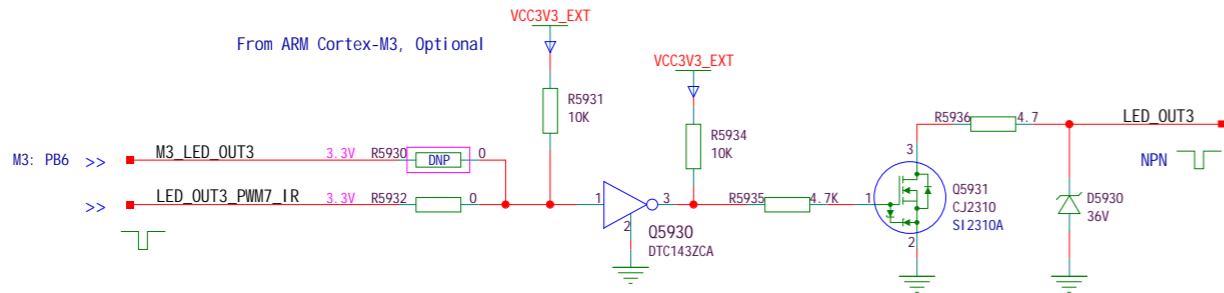
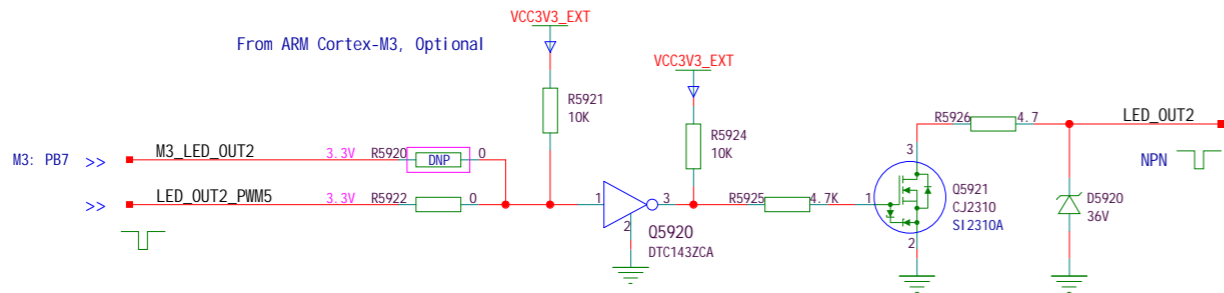
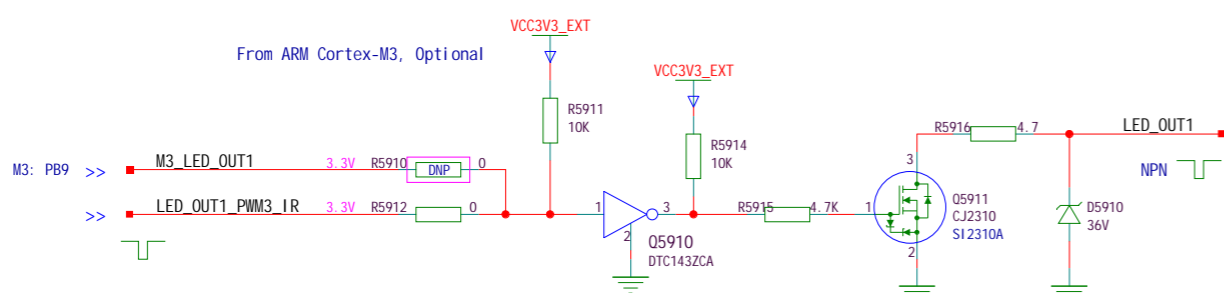
Dout for LED*3 and Buzzer, Relay*2



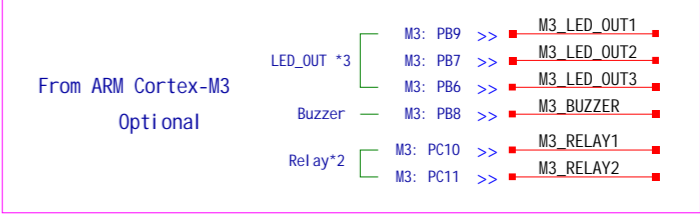
- LED_OUT1 TP5900
- LED_OUT2 TP5901
- LED_OUT3 TP5902
- +24V_OUT_LED TP5903
- BUZZER_OUT TP5904
- +24V_OUT_LED TP5905



- RELAY1 TP5906
- RELAY1_COM TP5907
- RELAY2 TP5908
- RELAY2_COM TP5909

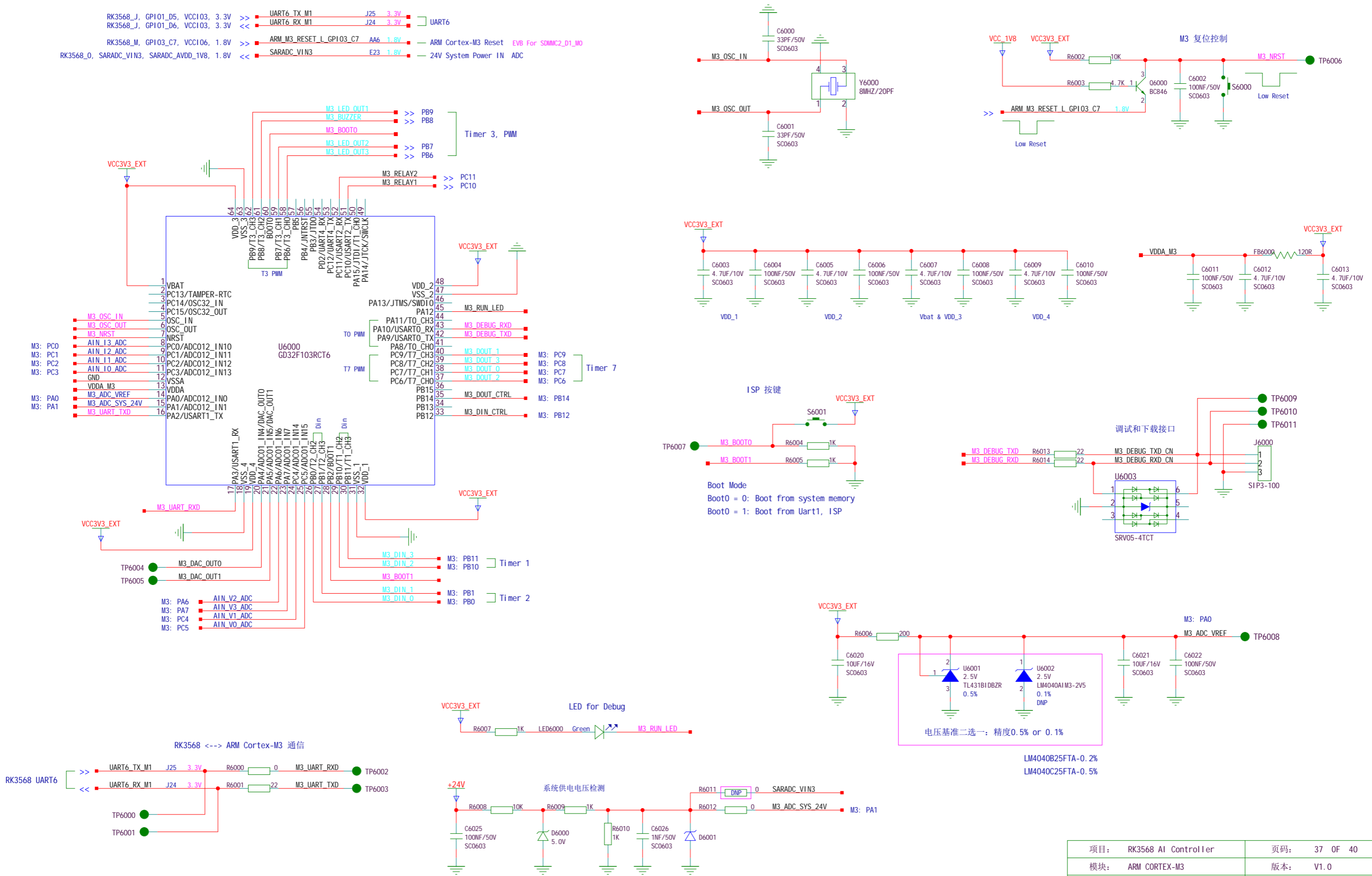


- From RK3568, Default
- RK3568_G, GPIO0_C2, PMU102, 3.3V
 - RK3568_G, GPIO0_C4, PMU102, 3.3V
 - RK3568_G, GPIO0_C6, PMU102, 3.3V
 - RK3568_L, GPIO3_C5, VCC105, 3.3V
 - RK3568_M, GPIO3_D4, VCC106, 1.8V
 - RK3568_M, GPIO3_D5, VCC106, 1.8V
- LED_OUT *3
- LED_OUT1_PWM3_IR AG23 3.3V
 - LED_OUT2_PWM5 AD21 3.3V
 - LED_OUT3_PWM7_IR AD20 3.3V
 - BUZZER_PWM15_IR_M0 AC2 3.3V
- Buzzer
- Relay*2
- RELAY1_L_GPIO3_D4 AA1 1.8V
 - RELAY2_L_GPIO3_D5 AA5 1.8V



项目:	RK3568 AI Controller	页码:	36 OF 40
模块:	DOUT FOR LED/BUZZER & RELAY	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

ARM Cortex-M3



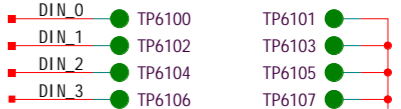
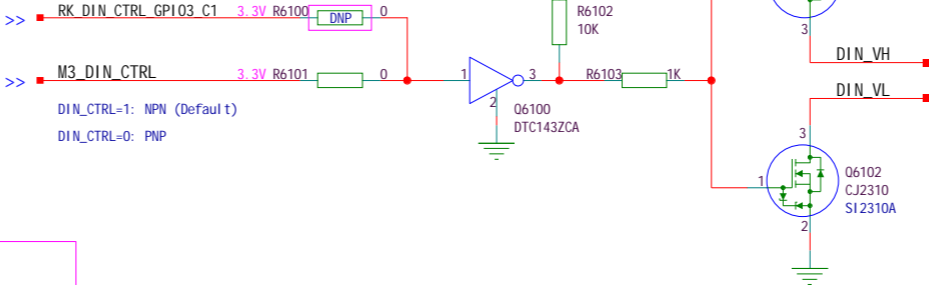
项目:	RK3568 AI Controller	页码:	37 OF 40
模块:	ARM CORTEX-M3	版本:	V1.0
设计:	Li Mngguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

Di n *4 Channels （ NPN/PNP ）

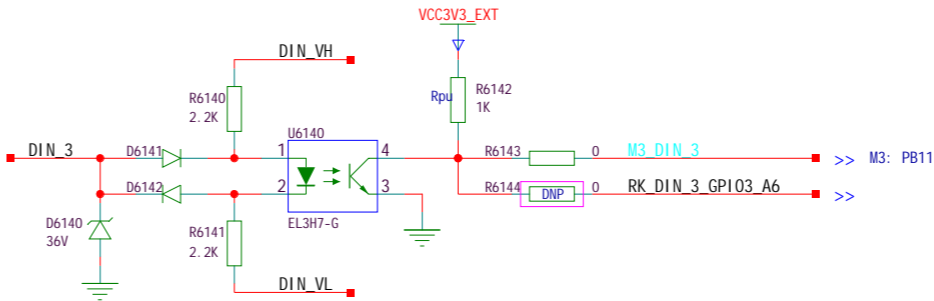
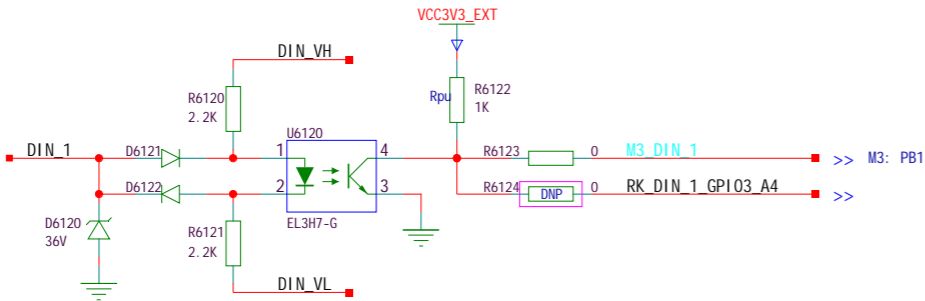
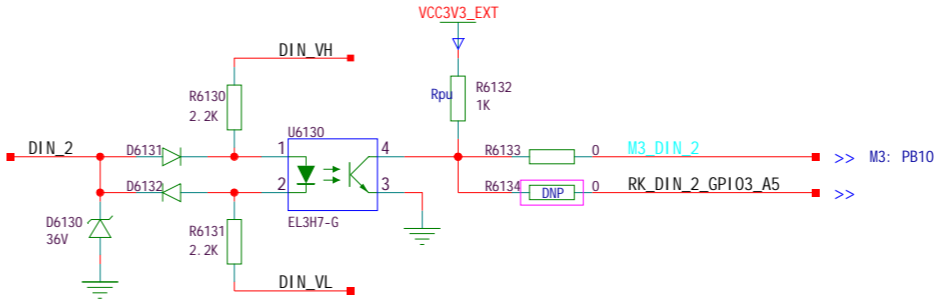
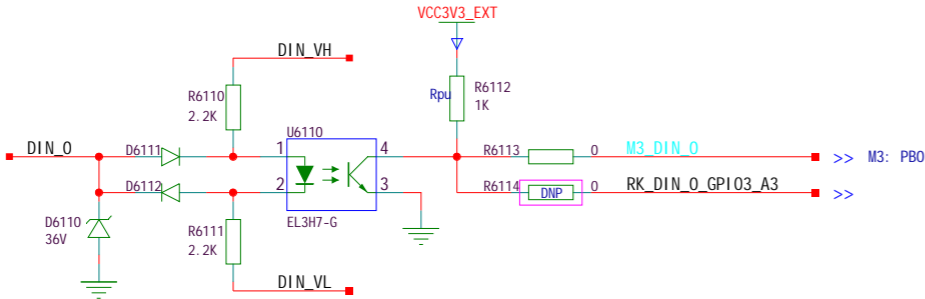
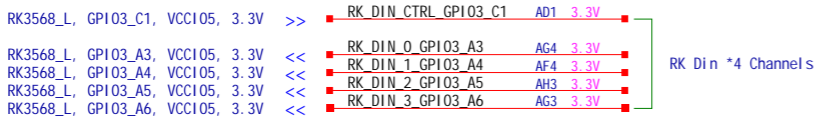
Din Control Logic					
DI Type	DIN_CTRL	PMOS (VH)	NMOS (HL)	DIN_VH	DIN_VL
PNP	0	OFF	ON	floating	GND
NPN	1 (Default)	ON	OFF	+24V	floating

Din Out Timing				
DI Type		下降沿	上升沿	
NPN		1uS	14uS	
PNP	24V	1uS	14uS	
	12V	2.5uS	14uS	
	6V	8uS	14uS	
				Rpu=4.7k, Tr=50uS Rpu=2.2k, Tr=25uS Rpu=1k, Tr=14uS

To ARM Cortex-M3, Default



To RK3568, Optional



项目:	RK3568 AI Controller	页码:	38 OF 40
模块:	DIN *4 CHANNELS	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

Dout *4 Channels (NPN/PNP)

Dout Control Logic						
Input	Dout Type	Dout_CTRL	Dout_CTRL_N	QH-b	QL-b	Dout
	PNP	0	1		0	
	NPN	1 (Default)	0	1		

From ARM Cortex-M3, Default

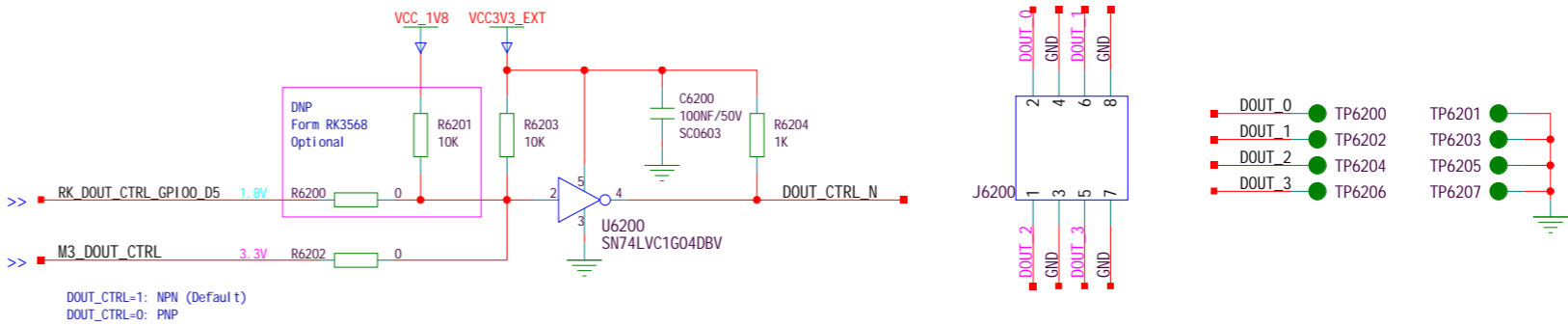
Dout Timing			
NPN, 2.2k Pull Up to DC24V	下降沿	上升沿	
	800nS	2uS	
PNP, 2.2k Pull Down to GND	上升沿	下降沿	
	500nS	10uS	

- M3: PB14 >> M3_DOUT_CTRL
- M3: PC7 >> M3_DOUT_0
- M3: PC9 >> M3_DOUT_1
- M3: PC6 >> M3_DOUT_2
- M3: PC8 >> M3_DOUT_3

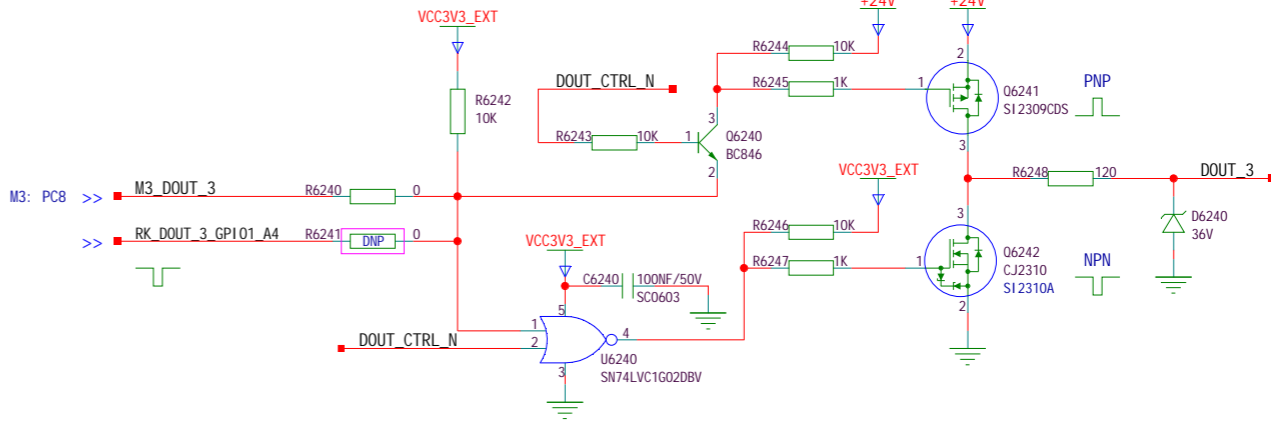
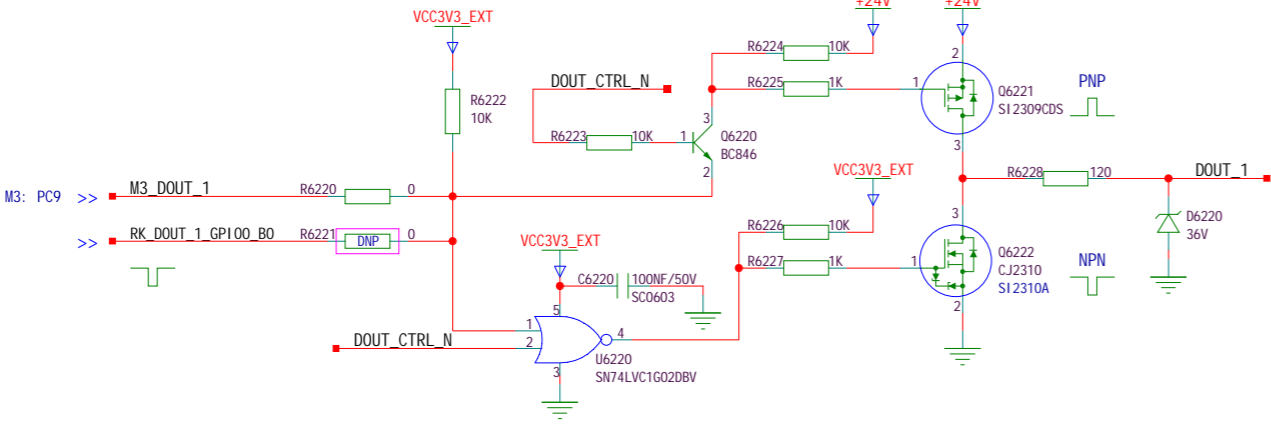
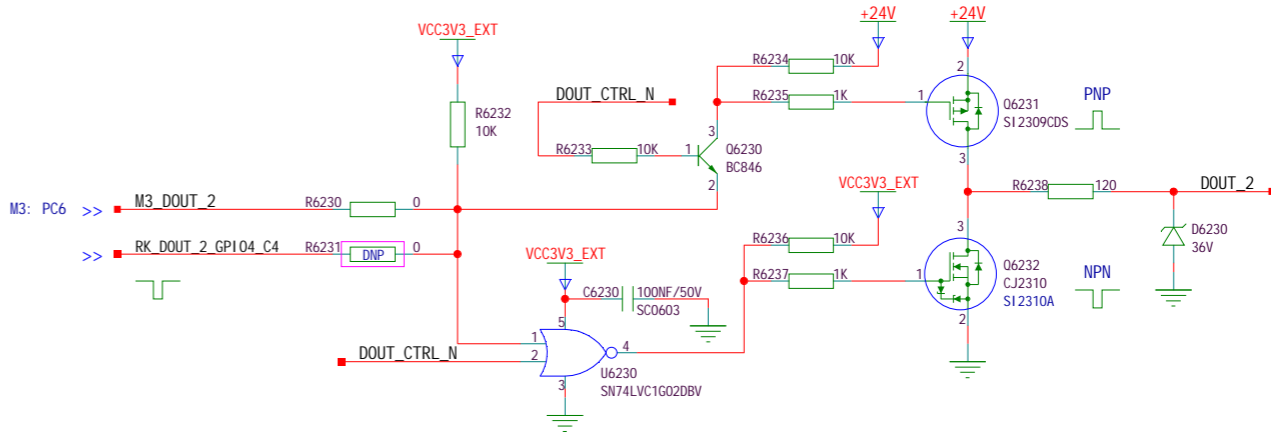
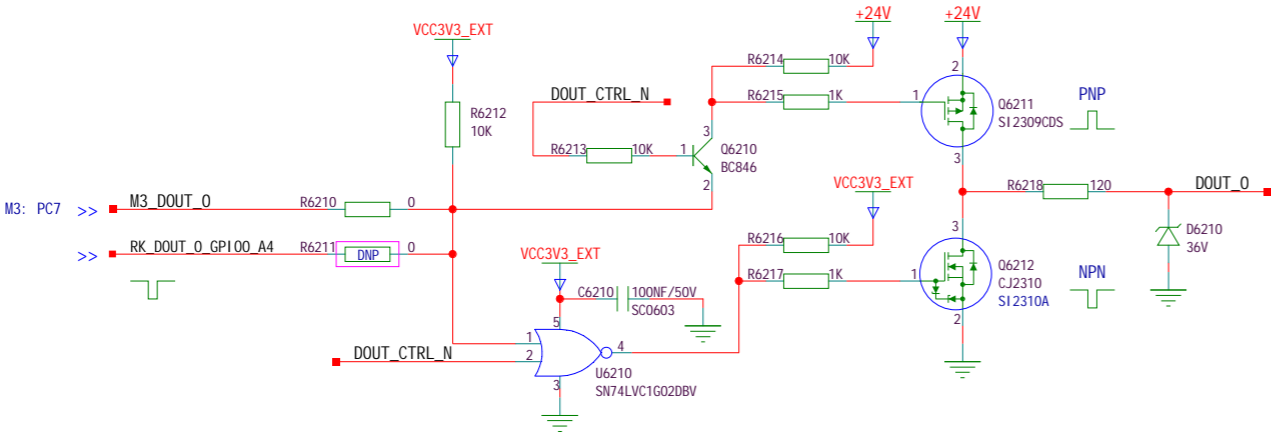
Form RK3568, Optional

- RK3568_G, GP100_D5, PMUPLL_AVDD_1V8, 1.8V >> RK_DOUT_CTRL_GP100_D5 AD25 1.8V
- RK3568_G, GP100_A4, PMU101, 3.3V >> RK_DOUT_0_GP100_A4 Y22 3.3V
- RK3568_G, GP100_B0, PMU102, 3.3V >> RK_DOUT_1_GP100_B0 AD23 3.3V
- RK3568_N, GP104_C4, VCC107, 3.3V >> RK_DOUT_2_GP104_C4 AH7 3.3V
- RK3568_H, GP101_A4, VCC101, 3.3V >> RK_DOUT_3_GP101_A4 F18 3.3V

RK Dout *4 Channels



- DOUT_0 TP6200 TP6201
- DOUT_1 TP6202 TP6203
- DOUT_2 TP6204 TP6205
- DOUT_3 TP6206 TP6207



项目:	RK3568 AI Controller	页码:	39 OF 40
模块:	DOUT *4 CHANNELS	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司

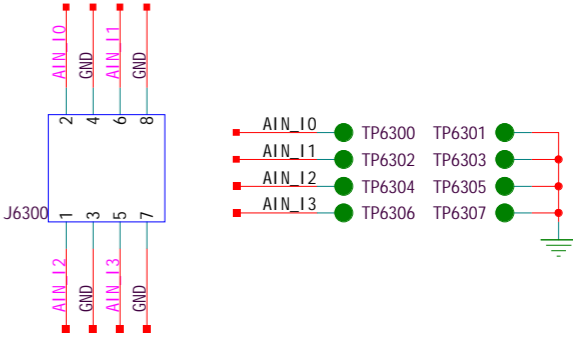
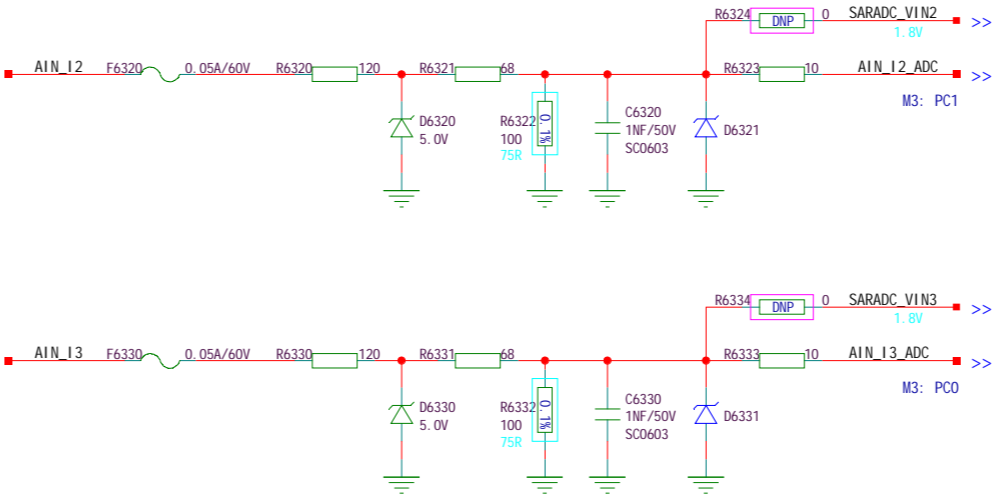
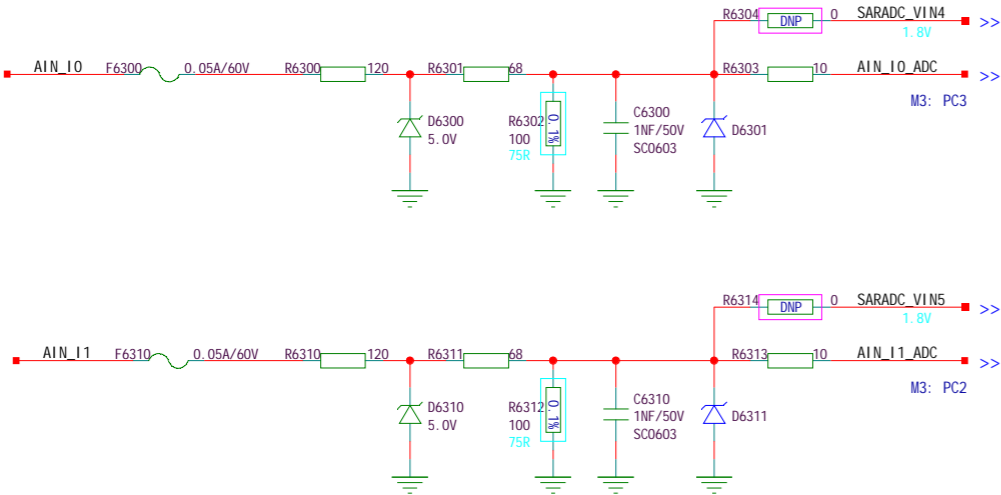
Ain: 4~20mA *4

M3: PC3 << AIN_I0_ADC 3.3V
M3: PC2 << AIN_I1_ADC 3.3V
M3: PC1 << AIN_I2_ADC 3.3V
M3: PC0 << AIN_I3_ADC 3.3V

To ARM Cortex-M3, Default

RK3568_0, SARADC_VIN4, SARADC_AVDD_1V8, 1.8V << SARADC_VIN4 1.8V
RK3568_0, SARADC_VIN5, SARADC_AVDD_1V8, 1.8V << SARADC_VIN5 1.8V
RK3568_0, SARADC_VIN2, SARADC_AVDD_1V8, 1.8V << SARADC_VIN2 1.8V
RK3568_0, SARADC_VIN3, SARADC_AVDD_1V8, 1.8V << SARADC_VIN3 1.8V

To RK3568, Optional



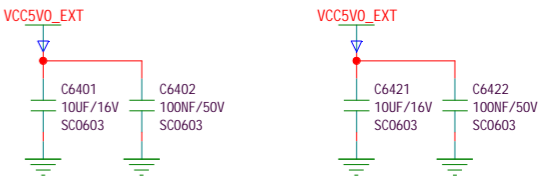
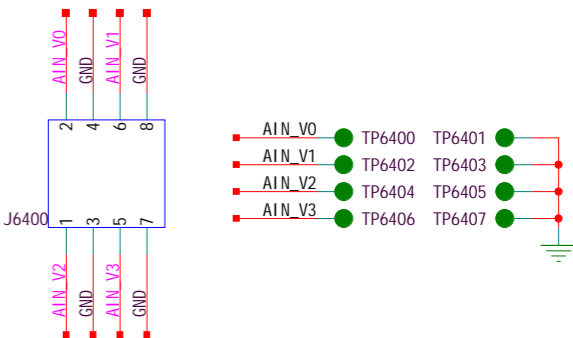
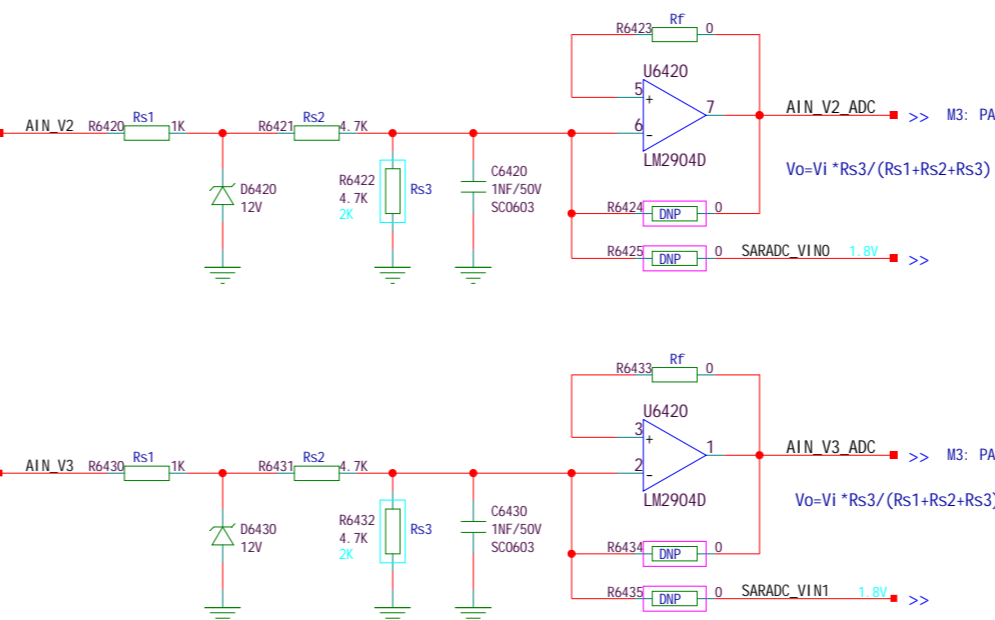
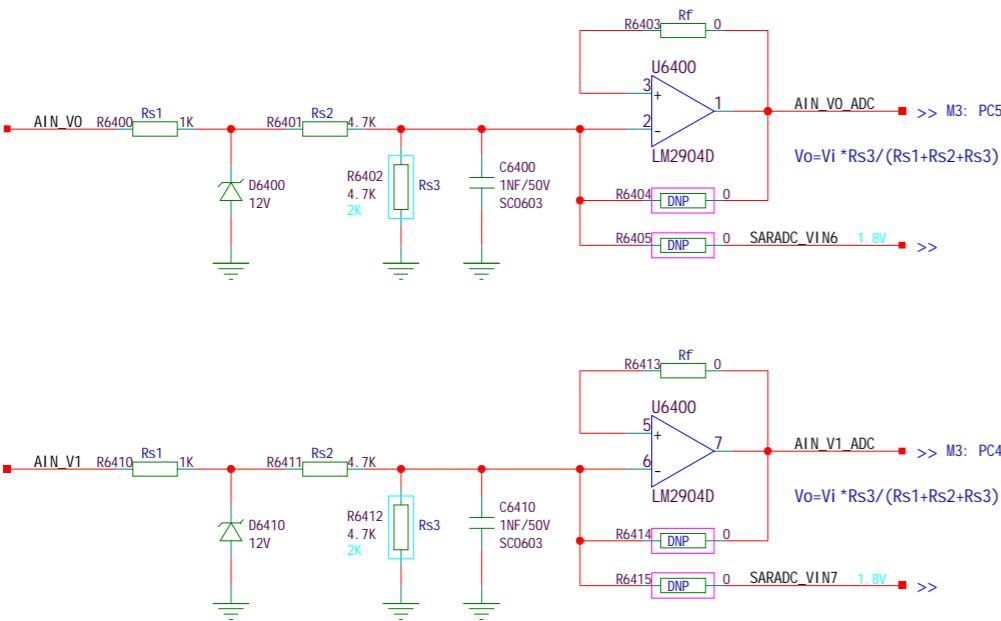
Ain: 0~5V *4

M3: PC5 << AIN_V0_ADC 3.3V
M3: PC4 << AIN_V1_ADC 3.3V
M3: PA6 << AIN_V2_ADC 3.3V
M3: PA7 << AIN_V3_ADC 3.3V

To ARM Cortex-M3, Default

RK3568_0, SARADC_VIN6, SARADC_AVDD_1V8, 1.8V << SARADC_VIN6 1.8V
RK3568_0, SARADC_VIN7, SARADC_AVDD_1V8, 1.8V << SARADC_VIN7 1.8V
RK3568_0, SARADC_VIN0, SARADC_AVDD_1V8, 1.8V << SARADC_VIN0 1.8V
RK3568_0, SARADC_VIN1, SARADC_AVDD_1V8, 1.8V << SARADC_VIN1 1.8V

To RK3568, Optional



项目:	RK3568 AI Controller	页码:	40 OF 40
模块:	AIN (4-20MA & 0-5V)	版本:	V1.0
设计:	Li Mingguo	日期:	2023.05.18
审核:	Ma Zhonggang		深圳市中科晟安科技有限公司